INFORMATION SOCIETY TECHNOLOGIES

(IST)

PROGRAMME

Contract for: Shared-cost RTD

Annex 1 - "Description of Work"

Project acronym: POET

Project full title: Power Optimisation of Embedded SysTems

Contract no.:

Related to other Contract no.:

Date of preparation of Annex

Proposal number: IST-2000-30125

Operative commencement date of contract:

1. Project Summary

1.1. Objectives

The main objective of the POET project is to develop a new design methodology and tool suite for power estimation and optimisation in heterogeneous embedded SoC designs. The key innovation of the approach is to enable design space exploration for low power system architectures, algorithm optimisations and system partitioning - from the earliest design steps seamlessly through to RT level (i.e. to the interface with standard industrial synthesis tools). The POET design framework will operate at each level of abstraction, i.e. algorithmic, hardware/software partition, cycle-accurate RT level. POET tools will manage and optimise all major contributors to power dissipation in large SoC designs such as ASICs, cores and processors, memories, communication and I/O interfaces.

1.2. Description of Work

The workplan is structured into eight workpackages (WP): six technical(WP1-6), one commercial(WP7), and one administrative(WP8). WP1 specifies the design flow for the development of low power integrated SoCs, defining the interfaces between the different power optimisation tools so they are able to interact seamlessly. WP2 develops methodologies to optimise power consumption of the software components of SoC design -- based on the power estimation techniques previously developed and enhanced in WP5. The SoC design outcome will be dependent on the architecture adopted in terms of processor and memory hierarchy, and on the compilation and operating system environment. WP3 deals with the development of methodologies and develops a prototype tool for interconnect and data manipulation. WP3 also develops the transfer and storage driven power optimisation of executable specifications of hardware units, including memory structures; these will be implemented using SystemC and C++. WP4 deals with the development of methodologies and prototype tools for power optimisation of memory sub-systems, and of the memory-processor and data-path communication interfaces. This enables automatic insertion of power management circuitry in cycle-accurate RT level descriptions, and automated synthesis of power managed RT level library macros. WP5 enhances the capabilities of power estimation tools already developed by Partners 1, 2 and 3 (partly in a previous ESPRIT project) so that the tools can interact fully with the new optimisation tools developed in WP2, WP3 and WP4. WP6 deals with the integration of the tools developed in POET, and with industrial evaluation of the tools in the application domains of the user partners. WP7 deals with both internal and external exploitation and commercialisation. WP8 deals with project co-ordination and management of POET, including financial and contractual administration.

1.3. Milestones and expected Results

Key milestones and results:

the preliminary and final versions of the different estimators and optimisers
integration of the POET tool chain
industrial evaluation of the tools
implementation of the exploitation plan

2. Project Objectives

The overall objective of the POET project is to address an increasingly limiting factor in system-level design – the control and design management of power consumption at all stages of the design process. Achieving integrated power management at the design-in level is becoming a key requirement for advanced silicon systems, and is increasingly necessary to enhance the competitiveness of the European silicon, communication and information processing industries.

Europe has strong and recognised capabilities in advanced SoC (Systems-on-Chip) design. As power management becomes *the* decisive factor in aspects of new ASIC design for certain new classes of products, especially small embedded and portable systems, it is becoming essential that European industry be able to mobilise new tools and methodology and compete with the best in the market. It is widely recognised that the leading EDA tools (Electronic Design Automation) mostly originate in the USA: the POET project intends to develop its tools and methodologies so they can be directly coupled with leading commercial EDA systems. This will enable us to develop and strengthen the excellent position of Europe in the area of system-level design tools, itself an emerging market where European companies have excellent opportunities. In turn, this will have a direct impact on European essential technologies and infrastructures for mobile communication and ubiquitous computing, as well as in the integration of both into integrated systems and services.

Current integrated digital Systems on Chip (SoC) designs pose new challenges to the development of a consistent and seamless design flow. The heterogeneous nature of various components of such systems (memories, IP programmable and non-programmable cores, glue logic) requires new design tools both for analysis and for optimisation. In particular, many of these systems find their application in the mobile domain, such as cellular phones, personal digital assistants and wireless Internet terminals. Therefore, there is an increasing demand from both semiconductor manufacturers and system houses for EDA tools that can help in addressing the power consumption problem during product development. Whilst significant research effort has been made in the recent past for studying and prototyping new computer-aided design solutions – both for power estimation and optimisation – the scenario of commercially available tools is still relatively poor. This is especially true at the highest levels of design abstraction, i.e. RTL (Register Transfer Level) and algorithm levels. In addition to hardware optimisation, embedded software design and instruction-level optimisation is quickly becoming more relevant. In the main, this is due to the co-design approach for many new designs coupled with the rapidly increasing presence of re-used and re-usable computational units and other logic blocks (e.g. CPU cores, DSPs, I/O and other micro-controllers) in contemporary digital applications.

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2.1. Main Objectives

Power dissipation is increasingly becoming a limiting factor in the integration of complex SoC (System-on-Chip) designs. This is starting to impact the mobility of ubiquitous computation and communication, as well as affecting the cost and reliability of communication systems and networks. Power management and reduction is most efficiently achieved at the system level, at the stage when algorithms are developed and partitioning is done. Experiments have shown that at one extreme, power reduction of several orders of magnitude can be achieved

between the best combination of algorithms and architecture versus non-optimised solutions. The POET project addresses this opportunity as its main objective – the development and integration of methodologies and tools for power estimation and optimisation of combined SW and HW descriptions of SoC systems. POET targets the algorithmic level for both hardware and software as well as the functional RT level of abstraction where power optimisations can offer the largest potential.
The various tools to be developed will operate at different levels of abstraction (including application-level software, algorithmic, cycle-accurate RTL) and will address all major contributors to power dissipation – especially in large SoC implementations. Since software and algorithm development of SoCs is mostly done in the C programming language, C will be directly supported as an input language for the system specification. The RT-level optimisation and interface to the back-end design flow will be based on VHDL so that it is consistent and compatible with the established silicon manufacturing design flow. In order to achieve these objectives, the following key activities will be addressed by the POET project:
Build and demonstrate a complete working design flow for power optimised SoCs from system specification to the RT synthesis level, showing significant reduction in overall design time and power reduction, with minimal overhead in terms of performance and silicon real estate.
Implementation of the design methodology in an efficient and integrated tool set, where not available commercially, in particular:

A prototype tool for power optimisation of C code specific to dedicated target platforms
A prototype tool for low power high level synthesis of designs with C-based specifications.
A prototype tool for power optimisation at the RT level of abstraction.
Evaluation and qualification of the project's results.
Augmentation of CAD product suites with innovative power design management software.

POET will also further develop and enhance the power analysis and estimation tools already developed by partners within a previous ESPRIT project. This will adapt them to the needs of an *integrated* environment required for advanced SoC designs, where estimation and optimisation must be carried out in an interleaved fashion throughout the design process.

2.2. Objectives per Partner

The relevance of the POET project also has direct commercial advantage to the project's participants:

OFFIS is extending its position in the high-level power estimation and optimisation domain.

CEFRIEL is consolidating its competence in power estimation and optimisation technology for embedded software.

POLITO is strengthening its position in the low power scientific community with particular focus on RT-Level estimation and optimisation.

ASEL gains commercial advantage by having access to the most advanced tools and methodologies for power optimisation of network switching and access systems, especially in customer premises and central office equipment in the ADSL and HFC (hybrid fibre coax) domain.

ARM is strengthening and consolidating its world-leading position in low power embedded cores by offering its customers a seamless tool flow for power optimised embedded software and core based architectures for embedded SoC designs.

OSC is extending its position in the European EDA market by offering advanced and integrated tools for the growing low power market.

2.3. Results

The principal results of the project will be:

Enhancement of various existing EDA tools and prototypes for hardware and software power **estimation** of embedded SoCs, usable at various stages of the design flow.
New EDA tools for hardware and software power **optimisation** of embedded SoCs.
Improved design capabilities of the user partners (ASEL and ARM).
Power optimised designs of the user partners, with attendant commercial advantage.
Dissemination of innovative research results within the community of IC and system designers.

3. Participant list

Participant Role	Participant Number	Participant Name	Participant Short Name	Country	Date enter Project	Date exit Project
C	1	Kuratorium OFFIS e.V.	OFFIS	Germany	Start of Project	End of Project
P	2	CEFRIEL	CEFRIEL	Italy	Start of Project	End of Project
P	3	Politecnico di Torino	POLITO	Italy	Start of Project	End of Project
P	4	Alcatel	ASEL	Germany	Start of Project	End of Project
P	5	ARM	ARM	United Kingdom	Start of Project	End of Project
P	6	OSC GmbH	OSC	Germany	Start of Project	End of Project

4. Contribution to Programme/Key Action

This proposal addresses Key Action IV, *Essential Technologies and Infrastructures*, Action Line 8, *Microelectronics – optoelectronics*, Task 8.1: *Microelectronics Design and Test*, Focus (ii) *Low Power design.* The proposal also contributes to Key Action IV, Action Line 8, Task 8.2: *Application-specific microelectronics* by *addressing tools and methods for embedded software especially towards low-power*.

The main objective of Key Action IV is to accelerate the take-up of technologies vital for the Information Society, and to broaden and deepen their field of application. As these general objectives state, some of the most promising but also most challenging opportunities are in the common usage of infrastructures for multiple applications, e.g. communication and its infrastructure, mobile information retrieval and ubiquitous computing. The POET proposal will enable design technologies particularly for power-sensitive mobile terminals and network infrastructure.

The POET project will contribute to the goals of the program by developing a tool-suite for fast, yet accurate power estimation and **optimisation** of designs, starting from high level abstraction down to the functional RT level. As power consumption is becoming a critical issue in the development of many digital systems, tools that allow designers to control and optimise the power budget during the various phases of the development process are in increasing demand. From an initial, system-level specification of the design, several partitioning/synthesis/estimation/optimisation steps are required to deliver a power-efficient architecture capable of meeting all the constraints posed at the specification stage. The required computational complexity for future mobile applications is increasing faster than the expected growth in DSP processing power (as predictable by Moore's Law). Consequently, combined HW/SW SoC designs will be needed to implement this class of systems. Also, it is clear that this computation power will then consume more electrical power. Without considerable improvements in power-optimised design techniques, the increase in power may be much larger than the predicted increase in battery capacity ('Ever-Ready' Law) and the natural reduction in power consumption resulting from smaller geometries and lower operating voltages.

Within this application area (and especially in 2G mobile phones) European suppliers hold a substantial share of the total world market. This is due in part to the advanced technological lead and know-how of the European industry in this domain. The ability to efficiently design microelectronic components with low power consumption is one of the most important enabling technologies for success in the fastest growing markets, such as integrated mobile computation and communication, and consumer equipment such as MP3 Players, PDAs and mobile phones. From a simplified viewpoint, the strong position of the communication industry in Europe is in contradiction to the small EDA industry in Europe. However, many of the more innovative EDA solutions – in particular for signal processing, HW/SW co-design, mixed-signal, and safety critical system design – have their origins in Europe due to the innovative strength of the European research community. Many tools have been developed in Europe, driven by industrial needs – in some cases partly with EU-funding. These have been productised by start-ups and brought to market either directly or through trade acquisition. The benefit to the system industry remains – access to tools which address European system design house needs.

POET's approach of power management designed-in rather than grafted on afterwards in expensive rework directly addresses the problem described in the 1999 Int. SIA Technology Roadmap: *"Better methods of accurate power prediction and analysis are more important than ever. Power prediction must be done as early and as accurately as possible in the design cycle, if possible at the architectural design phase. More and more applications have power budgets that cannot be exceeded for one reason or another, usually portability or reliability for a given package or system. Inaccurate power estimates often result in rework of the design architecture, logic, timing or sometimes costly rework of an analogue block, and results in delays in the design and lost market opportunity."*

5. Innovation

Modern integrated digital systems are characterised by complex and heterogeneous architectures, posing several new challenges to design flow development. The main challenge consists in the very diverse nature of the various elements of a system. Most digital Systems-on-Chip (SoCs) contain:

More than one, often several large-scale intellectual property (IP) cores such as data-processors (RISC cores, DSP data-parallel processors, dedicated functional units), micro-controllers, peripherals (PCI interfaces, serial and parallel drivers, external DRAM controllers, JTAG controllers, etc.)
A significant amount of memory in various forms and granularity levels, such as large DRAM banks, fast SRAM buffers, caches and register files, FLASH memories for non-volatile storage
Synthesised logic for interfacing large IP components and for supporting critical application-specific functionalities for which IP cores are either not available or inefficient
Other blocks, such as analogue components, sensors, and actuators, often operating in a mixed-signal domain

This heterogeneity shifts the design paradigm from classical “synthesis” to the most abstract task of *integration*. The use – and the relative assembly – of several pre-designed and pre-verified components (e.g. memories, and the IP blocks) is generally a more difficult, and less automatable, task than the translation of a consistent high-level description into a lower-level one, such as conventional RTL synthesis. For instance, the push for maximum reuse of IP components increases the importance of the optimisation potential contained in the *interfaces* between blocks, as well as that contained in their behaviour, as in the conventional approach. Classical hardware optimisation techniques are still important for the glue logic, needed for the interfaces between such blocks. Moreover, software is now a primary component of such systems, and the impact of software operations on the hardware can no longer be disregarded.

Computer-aided design frameworks developed in the past have focused on more homogeneous and conventional architectures, but the increasing need for design aids for heterogeneous SoCs prompts for a new generation of tightly integrated tools. These tools can help designers to both validate and optimise complex integrated systems, typically containing a large amount of memory, several IP cores and custom-synthesised application-specific logic.

Validation and optimisation of large systems on silicon have been studied extensively by the research community. The common approach taken in the past was to raise the abstraction level, in order to tackle system-level design issues as early as possible, usually in the initial phases of the design process and possibly even when functionality is still being specified together with design constraints. This approach has several advantages, but in particular it helps designers adopt a robust, top-down methodology, and to avoid major pitfalls early in the design process.

The output of system-level design tools is a partitioned specification, where part of the system functionality is implemented in software – to be executed by one or more processing elements – and part is assigned to dedicated hardware. Usually, software components are output in a high-level programming language (C, C++, Java, etc.), whilst hardware components are specified in a HDL (Verilog, VHDL). The common assumption is that the software and hardware components are processed separately by back-end tools, and only towards the end of the process are the end results of the software synthesis flow and the hardware synthesis flow merged and fed to a co-simulation engine for functional validation.

The main limitation of this approach is that it does not account for the complex (and often poorly understood) interdependencies between the different types of components in

heterogeneous hardware architectures early in the design flow. For instance, when synthesising software we need to avoid neglecting the requirements that the software execution imposes on the on-chip memory system and on the peripherals for off-chip memory access (for example, the allocation of data structures with respect to the memory architecture). Similarly, hardware specification and synthesis are heavily impacted by interfacing issues when the software is running on the core processors (for example, the locality of memory accesses). In general, it is not sensible to neglect the obvious fact that hardware and software interact directly, and that they compete for shares of a common power budget and limited silicon area. The interaction between system components has been a central issue in several recent initiatives in system level design. Design targets in performance, silicon area and power can be met only if a comprehensive view of the entire system is maintained – particularly as the design is processed from the system level down to lower abstraction levels.

This basic observation is at the foundation of the POET research effort. Our primary focus is on power consumption, its estimation and optimisation in large, heterogeneous SoCs. For this purpose, we plan to exploit some research effort developed in a previous ESPRIT project, that can be considered as the infrastructure for the proposed design methodology. In particular, we will re-use the technology provided by a set of power estimation tools applicable at different levels of design abstraction (namely, software, algorithmic and RTL), that should be used as analysis tools in the POET project.

The POET project is conceived with a three-fold objective: First, to enhance the available analysis and estimation tools, by adapting them to the needs of an integrated environment such as that of SoCs, where estimation and optimisation must carried out in an interleaved fashion. Secondly, to build a set of power optimisation methodologies and tools for heterogeneous SoCs. This objective represents the biggest challenge, because a suite of power optimisation tools that target such an environment can neither focus on a single level of abstraction nor consider a single contributor to the overall system power. Thirdly, to develop a low power system level design flow and to demonstrate the applicability, efficiency and quality of the tools on concrete industrial design cases from leading system houses and on most common platforms.

5.1. Design Flow

Currently low power design in practise means: low voltage, small feature size, clock gating, operand isolation, and power management. Clearly low voltage is a key influence on power reduction due to its quadratic impact on the power dissipation. However, there are limits due to reduced performance and increased leakage current. Further small feature size reduces the switched capacitance and hence significantly reduces power. Usually these parameters are not at the distinction of the designer and their positive effect are assumed in the power dissipation predictions of the roadmaps anyway. Other means at the gate and circuit level provide only power reductions in the area of some 10-20%.

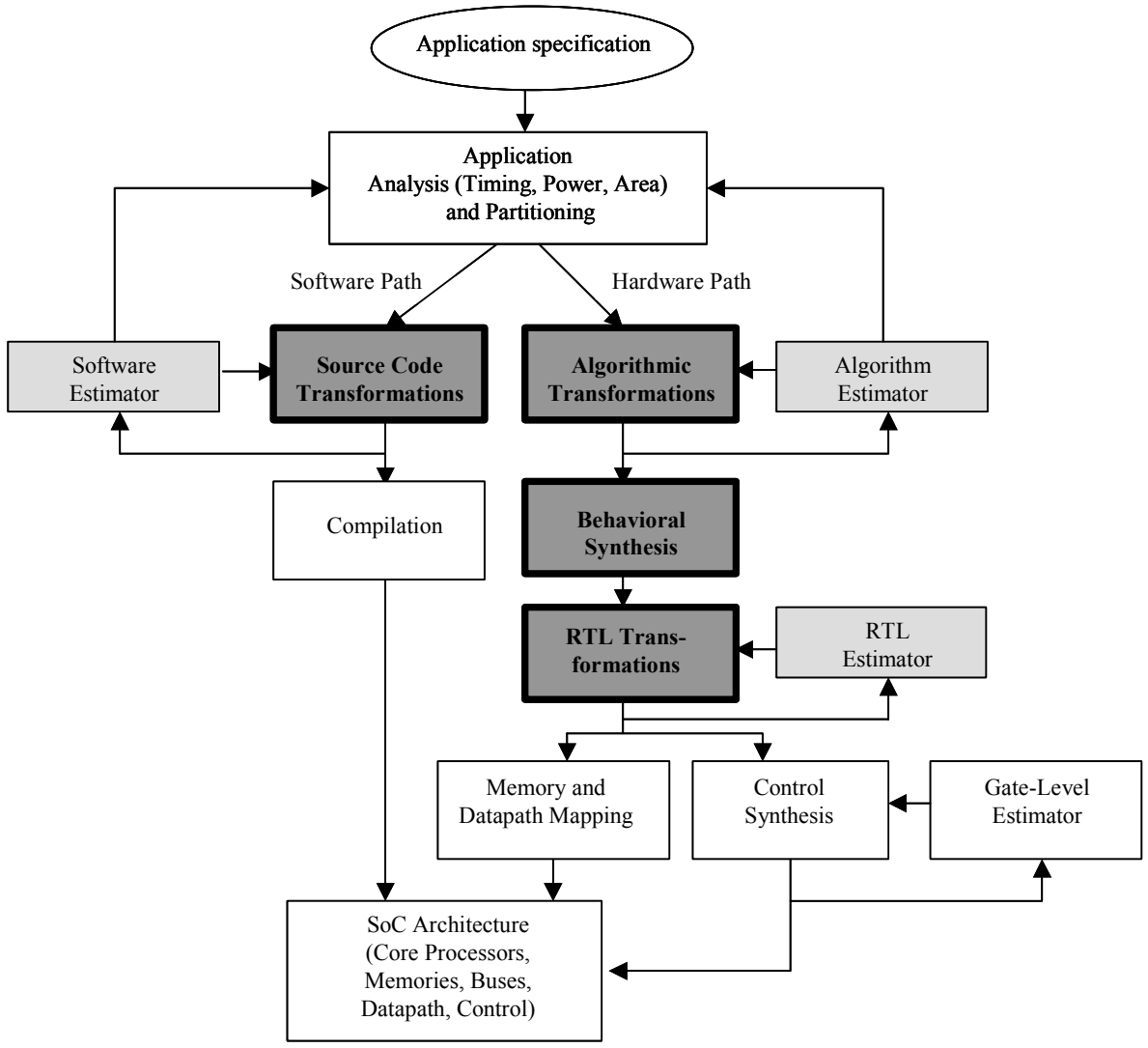


Figure 1: Proposed Design Flow for Power Estimation and Optimisation

Power estimation and optimisation at the system level, during software design and system architecture definition, have been addressed by prior research work. However, no seamless design flow approach through these levels - considering the main power drains - has been developed and applied so far. Within POET this flow will be defined driven by concrete product developments by the user partners ASEL and ARM. The flow will be coupled to industry standard commercial tools as far as available, and missing links in the tool chain will be developed by the research partners of the project (OFFIS, CEFRIEL and POLITO) and commercially made available by the EDA partner OSC.
For proper power analysis and optimisation, a full characterisation of the system components is needed. In order to minimise the time-consuming characterisation procedure, the number of libraries and technology files will be kept at a minimum. Figure 1 shows a preliminary design flow for power optimisation. dark grey boxes denote new developments in POET whilst light grey indicates parts of the design flow which already exist in prototype form and will be enhanced in POET to fully support the optimisation phases.

5.2. State of the Art: Design Tools

At the current time, there are no commercially available tools in existence which provide a comprehensive, integrated, multi-level design methodology for heterogeneous architectures.

There are a few stand-alone tools – mainly in the form of academic prototypes – that do exist, most of which target optimisation at a single, specific point in the design flow, as detailed later in this section.
Tools developed and integrated in the POET project will span several levels of abstraction and tackle all major contributors to power dissipation in large systems on silicon. To support this view, a power optimisation methodology is planned which spans three abstraction levels: *Software*, *algorithmic* and *cycle-accurate RTL*.

The software level concerns the software functions which run on the core/DSP processors. The output of POET will be the identification of design guidelines (at source level), tailored to reduce power requirements. Where practical, software transformations will be identified, which can be semi-automatically applied to existing application software at different levels of abstraction and stages of the synthesis flow. Prior the identification of the design strategy, an extensive analysis of the impact on power consumption of typical basic C-constructs and design templates will be carried out. In particular, the influence of data types, classes of operations and control structures on the overall power budget will be analysed. Other effects will be taken into account, such as the cross-interaction between the above basic elements, the presence of procedure calls and the use of dynamic memory. A suitable set of models and estimators will be identified to characterise the different aspects which influence code execution and related energy dissipation, including microprocessor-related power consumption of compiled code, data caching and data transfer, and application profiling. The methodology will be developed and tuned by consideration of a relevant set of real-world benchmark applications, to identify the typical kernels and software templates.

The algorithmic level refers to a functionally accurate algorithmic specification of the system. At this level of abstraction, the correspondence between operations and their execution time is not fully specified. Throughput, latency and synchronisation constraints are specified, however, and must therefore be taken into account during optimisation. The algorithmic specification can either be implemented in software, executing on a programmable processor, or be mapped onto dedicated hardware to be synthesised in later design steps. The decision on hardware-software partition is either left to the designer or to a higher-level design tool. It is assumed that the algorithmic specification contains specific annotations which specify the target mapping (hardware or software).

The cycle-accurate RTL refers to the conventional hardware description style used by designers in the synthesis domain. The main difference in terms of semantics – with respect to algorithmic descriptions – lies in the explicit notion of time that is assumed throughout the description. Operations happen between clock cycles, representing the smallest possible granularity. Another significant difference is represented by the type of simulation each description style can support – behavioural descriptions are purely functional (and therefore very fast), whereas cycle-accurate simulation requires synchronisation with a periodic time reference which determines the length of the simulation cycles. This cycle-accurate RTL differs from *structural* RTL, where the binding of synthetic operators to specific RTL library modules, such as adders and registers, is explicitly specified by means of the interconnection of the various blocks.
Two of the three main development activities in POET, carried out by CEFRIEL and OFFIS respectively, focus on algorithmic optimisations for software and for hardware. The third main development activity, lead by POLITO, targets the optimisation of power dissipation starting from a cycle-accurate specification. Algorithmic and cycle-accurate optimisations are intended to be carried in sequence, i.e. the former provides the input to the latter. It is important to emphasise that this two-phase optimisation approach does not take a partial view of the overall system power, but moves from a comprehensive view of all major contributors to the power budget. Approaches which do not account for all of these components may succeed only in reducing energy consumed in *part* of the system, which may only have a marginal impact on overall system power. More problematically, they may even increase overall power consumption by causing uncontrolled increase of power consumption in parts of the system

outside the optimisation scope (but which are tightly connected to the initial optimisation target).

5.3. Target Applications

The ASIC department of the Switching & Routing systems division of ASEL is working in the area of very advanced, high complexity ASICs on a large variety of telecommunication areas. This includes not only ASIC designs for ISDN and ATM switching products or cross-connect transmission systems, but also ASICs for access systems that are located at the central office or in customer premises equipment. In addition, the ASIC department has built up core competence knowledge in the area of embedded systems design and provides a configurable embedded processor platform to other ASIC design centres in terms of an intellectual property. This includes not only the VHDL and embedded software code, but also the provision of a methodology for using the processor platform within other designs, i.e. a compilation, synthesis, co-simulation, verification and test strategy. ASEL is in charge of extending its processor platform methodology to cover also low power design issues and tools, as low power is and becomes a crucial matter for ASIC designs throughout ASEL. ASEL especially sees the need for power estimation and optimisation tools that can be used very early in the design phase and that covers also the proportion of the power that is consumed by the software running on the embedded processor. Since modelling and simulation of complex ASIC with C/C++ models becomes more and more important and is already code of practise at many design centres of ASEL, power estimation and optimisation at this level is a key issue for making early trade-offs and an optimal HW/SW partitioning. As low power is a critical issue for all current and especially future designs, ASEL intends to drive the development and exploitation of tools in that area to make sure that actual and future requirements will be met. The developed tools and methodologies will be used in power critical projects to overcome the lack of commercial solutions. Furthermore ASEL will be able to spread the methodologies to other design centres via his processor platform.

ARM will apply the POET tools and methodology to the design characterisation of SoC designs which include an on-chip cache-based processor (as is typically found in most such designs). The implementation of the cache architecture and operation can have a substantial impact on the overall system power consumption – cache size and depth and hit/miss rates, write-buffering type and fetch block size, and cache-flushing decisions all impact the overall system power consumption, silicon area and performance to a considerable degree. In fact, non-optimal cache design can impact both performance and power consumption to a much greater degree than non-optimised core processor design alone. The POET approach will be used in later stages of the project to synthesise real applications with varying elements of cache architecture and implementation, to characterise the consequences for power consumption and performance in each instance. Application of these outcomes will then be used to optimise the design rules for cache architectures to achieve the best balance between the different requirements specified for the system.

6. Community added value and contribution to EU policies

The POET project proposal addresses the key vision statement of the IST 2000 workprogramme:

"Start creating the ambient intelligence landscape for seamless delivery of services and applications in Europe relying also upon test-beds and open source software, develop user-friendliness, and develop and converge the networking infrastructure in Europe to world-class".
The key enabling technologies for this vision are a wireless network infrastructure and the powerful mobile communication and computation terminals. Several of the WP2000 priorities to realise the vision are directly addressed by the POET project:

To improve natural and personalised interactions with IST applications and services. This includes multi-lingual/multi-modal interaction systems that are adaptable to the user's preferences and lifestyle (e.g. sensitivity to gender, age and culture).
To foster the development and convergence of networking infrastructures and architectures including the integration of fixed, mobile, on-line and broadcasting technologies.
To develop embedded technologies, their interconnections and their full integration into the service infrastructure, the workplace and business processes. To develop applications and services that take advantage of such systems.
To reconsider service provisioning in the context of any-where/any-time access to services and ambient dialogue modes including public services and, mediation and commercial transaction systems.

Further the proposal targets other objectives which strengthen the European industry and economy:

It promotes the take-up of methodology and tools in industrial environments, by solving problems and bottlenecks in several application domains.
It supports the development of design techniques that are useful and applicable to several application domains, in particular consumer and communication systems.
It contributes to the dissemination of such technologies to small, medium and large European companies, by offering direct marketing channels in Europe.

The vital importance of embedded systems for the telecom infrastructure has been generally acknowledged in the market. In our opinion, the project will substantially contribute to the implementation and evaluation of the above-mentioned objectives through the development of methods and tools to be used in the design of Systems-on-Chip (SoC).

The power consumption of SoCs is one of the main limitations of the integration of additional functionality. It has a massive impact on the reliability, power delivery, heat dissipation, package cost and battery life time. Hence means to reduce the power consumption of embedded SoCs have been identified as high priority research topics by the Int. 1999 SIA Technology Roadmap, the EDAA Design Technology Roadmap and by the CEC in the IST programme as well as by the special action ESD-LPD.

The embedded SoCs in communication systems (network and terminals) are complex architectures consisting of DSPs, µ-Controllers, memories, interconnect and dedicated hardware. Existing work on power reduction of these systems started at the component level by performing local optimisations. It is obvious that these optimisations cannot result in an overall optimised architecture. Attempts to start optimisation at the algorithm level for the software part have so far only been done on p-code or assembler level. Optimisations of behavioural descriptions of the hardware part and at the register transfer level are unique world wide. To tackle this challenge requires to focus the design scope and solution space to the most relevant application domains in the European market. The effort that is required for this proposal is suited for a project of European dimension. In fact, no single entity in one country could support the tasks of formalising, developing, promoting, AND applying the required methodology. Further in a previous EU-funded project the kernel of the consortium has very successfully demonstrated its good co-operation and the potential to develop low power tools driven by the specialised needs of some major European system houses.

NOKIA, the world wide market leader in wireless communication and Siemens ICN, a leading provider of network equipment have expressed their strong interest in this project and assured to help in the definition of the requirements and in the evaluation phase in a less formal way.

7. Contribution to Community social objectives

By providing an improved technology this proposal will contribute basically to improving employment availability of consumer products.

Unemployment is one of the key factors that needs to be reduced in the near future. In the last year, not only the less industrialised countries of the Community, but also the major and more developed ones, have suffered from high unemployment rates. Reducing unemployment requires maintaining a competitive edge of European products. Microelectronics and telecom are among the main industrial resources of the European Community and must be supported with this goal in mind.

Furthermore, according to a study conducted by GMM, the Microelectronics and Microsystems group of the German EE society, the semiconductor percentage content in consumer products will grow from 16% in 1999 to 22-30% in 2003. This growth implies that competitiveness in consumer products will become highly dependent on microelectronics development. Roughly speaking, each microelectronics employee influences 50-100 employees of the microelectronics client industries.

This will consequently favour the increase of the employment of young engineers and common labourers in existing design and production sites and will support the development of small and medium enterprises able to provide highly-specialised and niche services to the large companies involved in such design and implementation requirements.

Furthermore, market growth analysis shows that this project will especially benefit the semiconductor industries in Europe. In the competitive area in general purpose processors and peripheral chips, Europe has lost some ground in comparison with US and the Far East. However it is claimed that Europe is quite strong in the fields of ASICs (application-specific integrated circuits), algorithms and SW, as well as in system engineering. Due to the fact that most advanced algorithms and functionality in embedded systems will be carried on by ASICs, the market share can be increased by methodology and tools able to provide faster solutions and better quality of performances. Mobile and multimedia applications are expected to grow also considerably in the near future. Specifically it is claimed that data will account for 30% of network operators' revenue within two years. Due to the expected market expansion in this domain, microelectronic design improvements provided to European companies will allow an expansion of production and a resulting increase of the employment in these advanced sectors of society. ICE (Integrated Circuit Engineering) magazine 1998, predicts an average annual growth rate for the period 1997-2002 of 20% for ASICs and of 31% for Standard Cells, with a turnover (Bill. $) of 8.0 and 33.9 respectively, world-wide in 2002. The growth of telecommunication/industrial/consumer applications will be faster than that of computing. The support for these sections of the industry needs to be lead by Europe since it is where European strength lies.

Moreover these data prove that a turnover in microelectronics will enable a value addition in high level products, in particular in the European key industrial areas. It thus will enable employment in these domains. The design technology, methodology and tools developed in this project will also enhance the quality of life in several areas. New families of information technology products will be created and sustained in the areas of communication, consumer electronics, healthcare, information appliances, automotive electronics etc., promoting the ease by which citizens manage their everyday affairs. Furthermore, due to the significant potential of cost reduction that will be achieved using the accelerated design cycle, the aforementioned products will be made accessible to multitudes of citizens. Finally, these products will feature an enhanced quality and safety, due to the reusability of proven parts facilitated by our design methodology.

These economical and social opportunities, however, do not come for free. E.g. at this year's CO_2 conference in Amsterdam it was stated that:

20% of the electrical energy around Amsterdam is used for telecom.
In the US the internet is responsible for 8 to 9% of the total electricity consumption, including all computer applications this percentage grows to 13%.
It seems reasonable to predict that within two decades 30 to 50% of the nation's electricity supply will be required to meet the direct and indirect needs of the internet.

The transfer of 2,000 Kbytes of data through the net consumes the energy of a pound of coal.

While the information and communication society saves a lot of fossil energy because it avoids moving physical objects and reduces travel, it consumes a significant amount of energy itself. Hence besides the positive impact on the competitiveness of the European communication industry and the aforementioned impact on employment, the POET project helps to reduce the energy consumption of the information society and hence helps to protect our environment.

8. Economic development and S&T prospects

As explained in detail in the description of WP 7 of this Annex, the different exploitable results of this project will be:

A seamless design methodology for low power Systems-On-Chip (SoC) ranging from system level down to the RT-Level, that could be integrated in the co-design flow (if any) of any European electronic or telecom company.
A consistent suite of analysis, estimation and optimisation tools for different levels of abstraction in the design of low power SoCs.
A number of designs case studies done by the industrial partners leading to an evaluation report on the tools.

The specificity of our tools and their implied methodology will be of prime importance for a good market position of the future products.

8.1. Market Position

8.1.1. General Trends of the EDA Market (system and RT level)

EDA industry exhibits an average growth rate of 20.8 % per year, with strong discrepancies between subdomains: system level grows much faster (27.2 %), while traditional gate level design exhibits only 8% growth. This is still a global average. When going into more details, some specific tools are now on the decline (schematic capture, fault simulation). An interpretation to this may be that there is a very strong demand, facing a reasonably mature offer for design entry and simulation, while the offer for behavioural synthesis is still below customer's expectation. This means that there is room for new products in this field, even in a market that is strongly dominated by big companies (50% Synopsys, 30% Mentor).

8.1.1.1. Electronic System-Level (ESL) Methodology

In the SoC industry currently a shift towards system level design is noticeable. The discussions on C-based design is an obvious indicator. The technical and commercial background behind this move is threefold:

The total cost and performance of a system is primarily determined by the early design decisions done at system level, i.e. the algorithm selection and optimisation as well as the architecture definition. Figure 2 illustrates the relation between cost commitment and cost incurred during the design phases of a SoC. It is remarkable that the potential for cost and performance optimisation is very low at the late design phases.
The gap between technology improvements and design efficiency over time forces to concentrate on higher levels of abstraction. Figure 3 shows the respective chart of the 1999 Int. SIA Technology Roadmap. The move to higher levels of abstraction has taken place at similar situation in the past when cell based design and logic synthesis had been introduces. Finally related to the increase in complexity, the performance of tools of lower levels is insufficient to handle very large designs.
Finally related to the increase in complexity, the performance of tools of lower levels is insufficient to handle very large designs.

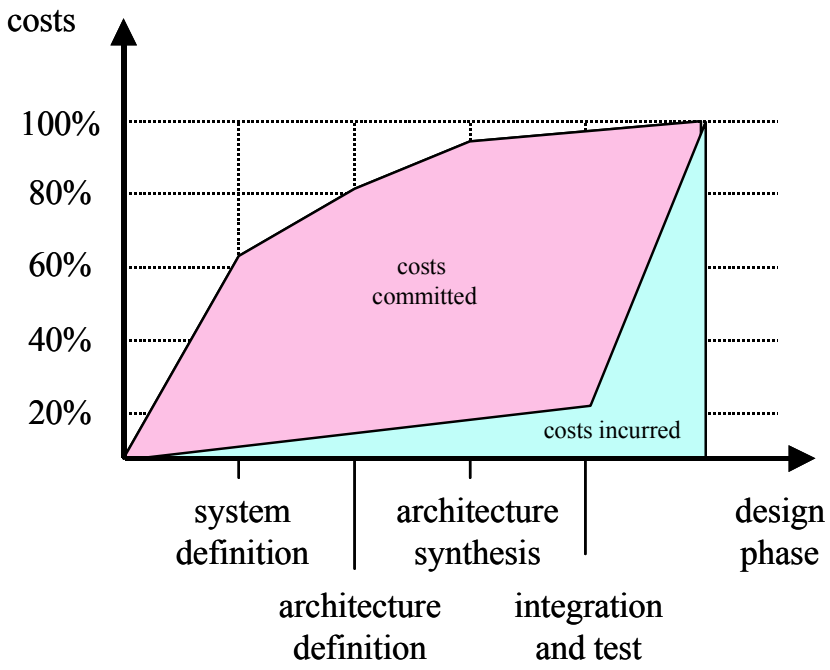


Figure 2: Cost commitment over design time.

These conclusions are supported by DataQuest market predictions. From the DataQuest ESL methodology classification, the following are relevant for the POET proposal:

Electronic System Level Design (ESLD)
Behavioural synthesis
Emulation and acceleration

The ESLD itself covers architecture synthesis and related tools. ESLD and behavioural synthesis and formal verification are „big hopes“, however, present solutions are not yet mature enough, and predictions are highly questionable. The market may grow much faster if more mature solutions are introduced (See Table 1 for details).

M US$ 1	1997	1998	1999	2000	2001	CAGR %
ESL	84.7	107.5	137.2	174.9	223.6	27.2
ESLD	42.3	50.8	60.9	73.1	87.8	20
Behavioural Synthesis	9.6	13.1	16	24.7	33.9	37.5
ESL Emulation and Acceleration	0.6	1.2	2.4	3.2	4.1	67

Table 1: Annual Turnover for EDA software by methodology

POET clearly targets at an increasing share of the EDA market, namely the ESLD market. The predicted growth in emulation and acceleration is a hint on the performance bottleneck in

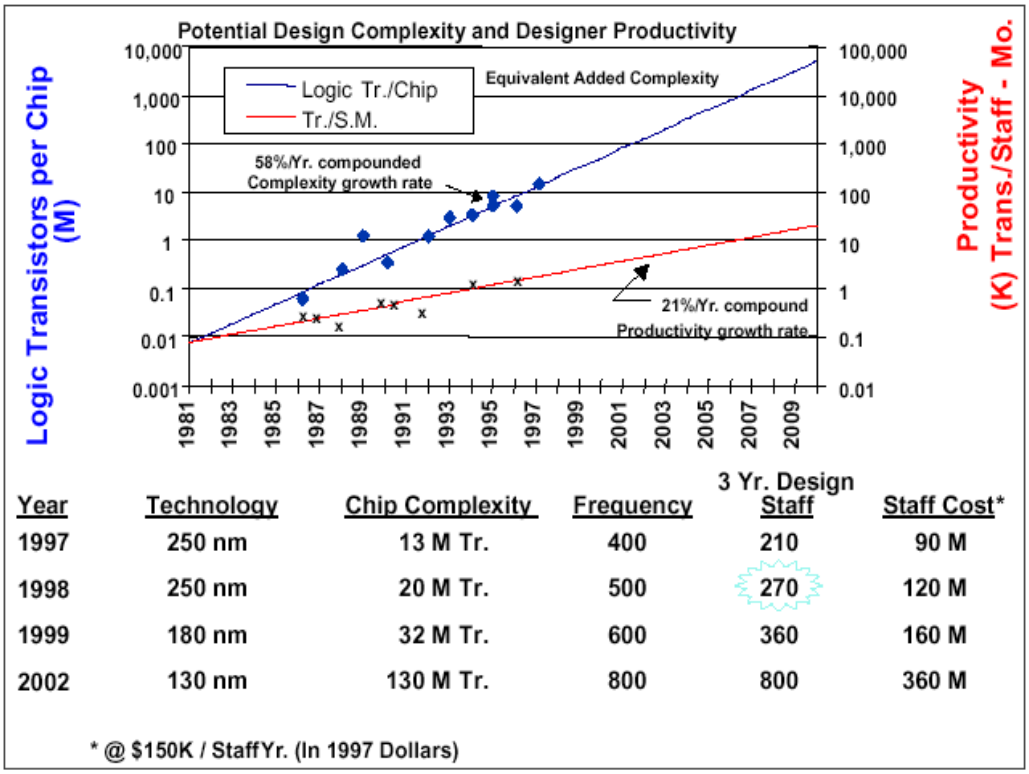


Figure 3: Design Gap (source: 1999 Int. SIA Technology Roadmap)

high level design evaluation and validation. No tools for power consideration at this level are on the market yet, hence POET clearly addresses a promising market niche.

RTL Methodology

RTL methodology was profoundly revisited under the pressure of sub-micron technology requirements. The dominant effect of wire delays and all other parasitic effects (electro-magnetic interference, metal migration, thermal problems) has pushed for a better link between RTL synthesis and library mapping with back-end related issues. Power is now an optimisation criterion as important as performance. A second issue is related to design methodology: embedded systems require appropriate facilities for HW/SW co-design. This has a direct influence on RTL design tools (co-simulation, RTL virtual prototype - emulation).

M US$	1997	1998	1999	2000	2001	CAGR %
RTL	697	896	992	1258	1585	23.1
RTL Design	28.7	35.8	39.7	44.1	49	13.7
RTL Simulation	303.4	368	404	484	574	18.5
RTL Synthesis	207.8	251.3	271	330.2	396.2	18
Target Compiler (layout generator)	9.4	16.7	20.9	26.1	32.6	34.1
DFT	50.2	51.5	57.7	83.7	121.3	28.5
Design Emulation and Acceleration	67.5	105.9	108	153.4	217.8	34
RTL Virtual Prototyping	5.8	10.6	11.2	23.9	31	44.3
RTL Analysis (power, timing, …)	39.7	56.3	79.9	113.8	162.7	42.1

Table 2: Annual Turnover for EDA software by RTL design task

As one can see in Table 2, one of the largest increases in turnover is expected to be in RTL analysis tools, in particular for low power.

8.1.2. Current Offer Low Power Tools at RT and Algorithm Level

In the following, we briefly review the relevant tool developments concerning high-level power optimisation. Given the context of the project, tools addressing the logic level and below will not be considered.

Software Level

Software power estimation techniques operating at different levels of abstraction have been proposed. Most of the approaches analyse the code at assembly level relying on an RT- or behavioural-level model of the microprocessor. These methods suffer two major drawbacks: the need of an accurate description of the microprocessor core and extremely long simulation run times. Recently, these problems have been partially overcome by focusing on an abstract (functional) model of the processor. Prototype tools implementing this technique have been developed within the PEOPLE project. The toolset provides core characterisation and assembly-level software estimation capabilities. No reliable and widely applicable strategies working at source-level have been proposed in literature and no commercial or prototype tools are currently available.

Concerning the power optimisation, many proposals focused on reducing the power consumed by memories, trying to minimize the need to access main memory through a careful management of data organisation, while exploiting the presence of caches. Other techniques operate at the instruction-level, and are based on a proper modelling of the microprocessor to provide power figures for each instruction. Power optimisation is then accomplished by selecting the best mix of instructions to execute the given application. A few techniques, still working on the code, for specific classes of applications can reduce power

demand by decreasing the accuracy of computation within the limit of tolerability. Dynamic variable-voltage techniques have been also proposed, to reduce performance and power consumption, during the execution of weakly critical sub-tasks. Dynamic power management can be also employed at system level, by means of a suitable methodology forcing (sleep) low power states, when the system becomes inactive; both fixed and predictive strategies have been proposed.

Hence, the task of managing the software-specific power-issues is not yet shifted toward EDA vendors. In particular, there is a lack of methodologies and tools working at source level both for estimation and optimisation of power consumption.

Algorithm Level

The research and development centre IMEC, Belgium, has developed a system level synthesis tool called Matisse. Matisse transforms a concurrent object-oriented system description into synthesisable hardware respectively compilable software descriptions. The focus of the design space exploration in Matisse is on the memory management and the memory architecture. Power models of the memories and the memory managers are applied. However, only constant external I/O load is assumed which limits the accuracy of the estimated communication cost. The power consumption of the address generating logic is not considered.

ATOMIUM, another tool from IMEC, allows a design space exploration for data storage and transfer dominated multimedia designs written in C/C++. Also in this tool, the power consumption of the memories is included in the cost function but all other power contributors are not taken into account. Basically, power is minimised by removing redundant memory accesses and splitting memories to avoid multi-port memories.
The Behavioural Compiler from Synopsys allows insertion of clock gating logic while compiling a behavioural description to the structural RTL level. Other power optimising features are not included.

PowerBuster-D from ASC synthesises behavioural HDL designs into structural RTL with the objective of minimizing power consumption under a performance constraint. Area of the design can be treated as either a constraint, or an optimisation parameter, along with power. The tool can also determine the optimal clock period for the design. PowerBuster produces and RTL datapath instantiating selected RTL library components, and an FSM controller for the datapath. The output of PowerBuster-D is compatible with popular RTL synthesis tools. This project is developed in collaboration with a university and seems to be stopped. It may restart in the future if a new partner gives founding for new development and industrialisation of the tools. The level of beta support evaluation is unclear at the moment. It is not clear which synthesisable sub-set PowerBuster supports.

Register Transfer Level

Power Compiler from Synopsys addresses power optimisation at the RTL by resorting to two distinct techniques: Clock gating and operand isolation. Clock gating circuitry, although automatically inserted in the RTL description, is only exploited during RTL-to-gate compilation; therefore, it can not be seen as a pure RTL optimisation solution (synthesis is required). Operand isolation can not be considered as an automatic RTL transformation, at least in its current implementation within PowerCompiler. In fact, the designer is required to manually identify the data-path blocks whose operands should be isolated and to mark them with pragmas in the VHDL/Verilog code, so that during synthesis useless computations are avoided. The most sophisticated and effective optimisations supported by PowerCompiler take place at the gate-level; therefore, PowerCompiler cannot be considered a real competitor of the RTL optimiser that will be developed within POET, whose target is rather the cycle-accurate RTL.

WattSmith from Sequence identifies power optimisation opportunities at the functional RT level. Optimisation opportunities like ignored memory reads or explicit clock enables which might be replaced by a gated clock are detected. WattSmith can thus be considered as an "advisor" for the designer; in other words, its main purpose is that of pointing out to the designer what kind of optimisation can be applied to some blocks of the description; however, a lot of human intervention is required to perform the optimisation in practice. On the contrary, the POET RTL optimiser will provide push-button optimisation capabilities. Furthermore, it will exploit more innovative (and potentially effective) techniques for power minimisation ("local" optimisations, such as those proposed by WattSmith, will be paired by more "global" optimisation, e.g., synthesis of the memory hierarchy, including caches, systems bus interfacing, global power management).

8.1.3. POET's Unique Feature: A Seamless Low Power SoC-Design Flow

System-on-Chip (SoC) design flows, as they are applied by many design companies, commonly start with a C/C++ executable specification of the system's functionality. An in-depth analysis of the specification is carried out to get a rough estimate of the timing behaviour as well as area and power requirements. Based on these estimates, the system description is partitioned into software and hardware parts. The software parts are mapped onto processors and DSPs while the hardware part is synthesised to a gate level netlist. Timing and overall system cost are the driving metrics for this partitioning step.

After partitioning, the POET low power optimisation methodology is applicable. This methodology will be realised by a set of new design tools. The software power optimisation flow transforms the software specification into a functional equivalent description. The resulting description is optimised with respect to the required energy consumption to execute on a given processor architecture including the memory sub-system. Traditional compilation finishes this part of the design flow.

The hardware specification is optimised for its power consumption at two different levels of abstraction in order to benefit from all effective optimisation design tricks. At the algorithm level, the hardware specification is first transformed similar to the optimisation step at the software side. However, the hardware transformations have a different cost metric behind. These transformations are mainly interconnect driven because interconnect cost tend to dominate the overall hardware power cost. The second design step at the algorithm level is synthesis to the register transfer level of abstraction. This high-level synthesis task is supported by the POET design flow in that low power scheduling, allocation, and binding constraints are generated.

Finally, fine-grained power optimisations at the RT level are performed which address communication interfaces, power management, and the memory hierarchy. Logic synthesis and place and route, being outside the scope of POET, are the remaining design steps.

8.2. Consortium Exploitation plan

A workpackage (WP) has been identified with the purpose of defining and initiating the exploitation of the project results by the consortium (see description of WP 7 in Part B of this proposal). As the EDA company of the consortium, OSC, will be responsible for the management of this WP. The exploitation effort will be undertaken by all of the partners, each with their specific interests and missions:
The end-user companies, ASEL, and ARM will internally use the methodology and tools defined in this project, and will contribute to the external promotion of the project by publishing their experience as users.
The industrial partner ARM will utilise the tool developments to strengthen its offer in design support for low power applications.

The EDA company OSC, together with the subcontractor BullDAST, will assure the external promotion of the tools developed within this project, and will define a strategy to industrialise and market EDA products based on these tool prototypes.
The research institutes OFFIS, Politecnico di Torino and CEFRIEL will actively support the external promotion of the methodology and tools of this project by presenting papers and contributing to demos of prototype tools at various conferences and exhibitions.
Associated industrial parties include Siemens ICN and Nokia will evaluate the results and if efficient will internally exploit them. See the included letters of interest at the end of this document.

As detailed in the description of WP 7, the important milestones for the consortium exploitation will be the tool demonstrations during EDA conferences and exhibitions, such as the Design Automation and Test in Europe (DATE) conference and exhibition, the Asian-Pacific-DAC (ASP-DAC) exhibition and conference in Asia and possibly the Design Automation Conference (DAC) in the US. Other common promotion actions, such as publications and WWW advertising, will be undertaken during the project. The estimated costs of these exhibitions and actions for OSC are stated in "Other Specific project Costs" on form A4.

Politecnico di Torino, CEFRIEL and OFFIS have a history of successful joint collaboration, especially in the area of low power design and tools. This co-operation will be extended to the spin-offs OSC and BullDAST. Respective co-operation agreements between the institutes and their spin-offs are in place.

This unique synergy and close co-operation between EDA vendors and research institutes will permit the full exploitation of the project results at the different levels mentioned above. The research institutes will promote the new low power design methodology, as well as the tool suite, by publishing articles in international conferences and organising tutorials on the tools. OSC and BullDAST will use their existing links into industry to directly market and build up new links directly and through joint marketing agreements as well as through international distributors to market the tool suite.

8.3. Individual Exploitation plans

The project is clearly driven by industrial partners, each of them investing 50% of the project cost from their own budget. It is hence the prime commercial objective of each partner, to receive a return on their investment as soon as possible. The appearance of this return, however, may be of a completely different nature for each partner. In some cases, the project results will put the partner in a favourable position with respect to the competition because of the experience with and access to advanced design technologies and tools. In other cases, the designed prototypes will be directly engineered into marketable products, e.g., for the EDA market. Finally, the results may be exploited as a starting point for future research activities or key technology for spin-off companies. The following sections describe the individual exploitation plans and expectations for each partner.

8.3.1. OFFIS

Since direct marketing of tools is beyond the scope of OFFIS, being a non-profit research institute, OFFIS will rely on OSC as a marketing channel of the tool set. OFFIS will transfer the know-how and the right for non-exclusive unlimited exploitation under a licensing agreement with OSC to allow them to market the POET tools. This exploitation channel is actively supported by OFFIS technology transfer activities as outlined below.

In the previous PEOPLE project, OFFIS has developed prototype tools for power estimation at the behavioural level. These tools have been packaged together with power estimation of memory usage and power characterisation tools as well as with a graphical user interface under the registered trade mark ORINOCO®. Parts of the ORINOCO® algorithms have been

registered for patent. For OFFIS as a research institute, the consolidation of its low power design technology and amendment by optimisation tools as well as the feed back from industrial applications on the feasibility, the efficiency and the limitations is very important.

By developing, implementing and maintaining the ORINOCO® tool suite, OFFIS pursues the following objectives:
The know-how of low power SoC design and optimisation will be integrated into courses at Oldenburg University, which is closely connected to OFFIS (e.g., lectures on embedded system design). In this way, students will have the opportunity to get in touch with this new modelling paradigm.

Similarly the know-how will be integrated into low power design courses offered at the OFFIS Training Centre (OTC) possibly in close marketing co-operation with the Mikroelektronik Akademie, Hannover, a subsidiary of the former Sican Design Centre.

Usage of the experience and tools in the OFFIS Design Centre (ODC) which is currently being founded. The target application domain of ODC is low power communication systems, for which power optimisation is crucial. Hence OFFIS aims at putting itself into a favourable position also in the design service business by applying the results of the POET project including the whole POET low power design flow.

Consolidation of OFFIS as a competence centre for design methodology and tools for low power SoCs.

To reach this objective, OFFIS actively publishes and promotes its low power technology. In recent years ORINOCO® has been presented at several international conferences and exhibitions (e.g., ISLPED'99, ISLPED'2000, DATE'99, DATE 2000, DAC 2000). OFFIS has begun to organise hands-on workshops in order to give the participants an idea of the benefits and quality of the ORINOCO® tools. These activities will be continued in the future.

OFFIS relies on OSC to market the ORINOCO® power estimation and optimisation tools.

8.3.2. ASEL

ASEL is working in the area of very advanced, high complexity ASICs. Thus low power is expected to be a crucial issue for all future activities. ASEL intends to drive the development and exploitation of tools in that area to make sure that actual and future requirements will be met. The developed tools and methods will be used in power critical projects to overcome the lack of commercial solutions.
The company foresees that power will be a crucial factor in the design and implementation in new generation ASICs (Systems on silicon). For this reason ASEL feels that is of enormous importance to utilise the estimators and optimisers developed in the POET project.
The exploitation of the results during POET Project life-span will be the application of the tools to the design of a complex device. Some simpler modules will be considered as benchmark to provide feedbacks to the developers. The complexity of the device will be representative of ASEL's internal needs. The benefit and advantages offered by the technology will be evaluated thoroughly. After a positive testing and acceptance of the tools, internal qualification will be granted. In this case the exploitation will proceed after the end of the project with the integration of the tools in ASEL proprietary design flow. Furthermore ASEL will organise seminars and training courses regarding power estimation and optimisation to improve the internal dissemination process. The commercialisation of EDA tools being outside the strategic commitment of the Company, no policy will be applied in this field.

8.3.3. ARM

The Low power design tools developed in the POET project will enable current and planned ARM architectures to achieve the performance requirements of current and future mobile applications. It will generate incremental revenue for ARM through allowing it to address new markets, produce cost reduced versions of existing applications and to develop higher performance, next generation applications. As a leading provider of microprocessor core for power sensitive applications it is vital to enable designers to evaluate both processor and system architecture choices and their impact of final system power before committing to silicon. As the complexity of designs increases the ability to perform these complex calculations requires tools support. The availability of these tools is therefore critical to ensure the successful implementation of ARM based design and hence the profitability of ARM.

8.3.4. CEFRIEL

CEFRIEL being a research centre subcontracts the promotion and commercial exploitation of their prototype tools to BullDAST. CEFRIEL will do dissemination of the results of the project through several channels in order to provide the maximum international visibility to the achievements. Technical articles and presentations during international conferences and workshops addressing system-level design and low power issues will be provided (as happened for the PEOPLE project), with some extent during exhibits in which OSC/BullDAST will have a booth. Seminars and training initiatives will be triggered to get feedbacks and promote the use of our tools and methodologies by including it as part of the Master Program in Information Technology provided by CEFRIEL, that is also open to designers coming from the over 20 main industries sponsoring CEFRIEL, representing the major players in the field of Communication and Information Technology. This will represent an additional important vehicle to promote and consolidate the relationships with such industries and to directly show, with the necessary extent, the potential benefits of the POET methodologies and tools directly to the industrial end-users.

8.3.5. OSC

Being a system level EDA vendor for embedded systems, OSC will naturally concentrate its exploitation efforts on the software technology and the tools developed within the project, i.e., the SW-power-estimator and optimiser (developed by CEFRIEL), ORINOCO® (developed by OFFIS), and the RT-level power optimiser (developed by Politecnico di Torino).

The business unit “Embedded Systems” in OSC is currently offering a suite of tools for formal verification of embedded systems. These tools originate from research at Oldenburg University and OFFIS. The tools have been transferred for exploitation to OSC under a co-operation and licensing contract. OSC is responsible for the further development, integration, support, training and marketing of the verification tools. The marketing is done through a joint marketing agreement with i-Logix, the vendor of the Statemate and Rapsody tools. Customers of the OSC verification tools include: BMW, Daimler Chrysler, General Motors, Nissan and PSA.

This agreement and marketing strategy is a model for the exploitation of the POET tools.

OSC is currently extending its portfolio of products by tools for system level design of communication systems. OSC is preparing the marketing of the ORINOCO® tools, which will be licensed from OFFIS and industrialised. The ORINOCO® tools have been presented at DAC’99, at DAC 2000, at DATE 2000 and at the Int. Symposium on Low Power Electronics and Design (ISLPED) 2000. During these demos they gained a lot of interest which led to on-site presentations at Bosch, IMEC, Infineon, Nokia and Philips. Currently evaluations are being performed at IMEC, the ORINOCO® technology is in use at Bosch other evaluations are

scheduled for early 2001. At the 38th DAC, June 2001, ORINOCO® will be shown at the joint OSC / OFFIS booth.

In view of the predicted growth of this market segment and the fact that the POET tools cover the entire system level low power design flow in a new and seamless way which is currently without any competition on the market place, OSC “Embedded Systems” expects to increase its revenue by several millions of EUROs by addressing the communication industry and selling licenses to the major players.

8.3.6. Politecnico di Torino

As a public university, Politecnico di Torino is not in the position of marketing and industrially exploiting the results of any research project. For this reason, a spin-off company (BullDAST) has been established in year 2000 with the major purpose of turning into products the prototype EDA tools that have been developed over the years by the EDA group. BullDAST will support OSC in the commercial exploitation of the POET results which are directly related to the activities covered by Politecnico di Torino.

The main contribution of Politecnico di Torino to the exploitation of the POET project will be on the dissemination of the achieved research results through technical presentations at international conferences and workshops, technical articles in the major journals and magazines addressing system-design and low power design issues, participation to fairs and exhibits such as those held at DATE, DAC and ISLPED, lectures and seminars in the context of international schools (e.g., Master programs in European universities, NATO summer schools) and training initiatives (e.g., EuroTraining courses).
Similar dissemination has distinctively characterized the exploitation activities carried out by Politecnico di Torino within the PEOPLE project. A total of 13 journal/conference articles (including contributions on IEEE Trans. On VLSI Systems, DAC: Design Automation Conf., ICCAD: Intl. Conf. On CAD, ISLPED: Intl. Symp. On Low Power Electronics and Design) have been published on subjects directly related to the results achieved in PEOPLE. Most of the research findings from the project are also included in the list of contents of the course: “Design Techniques and Tools for Low power Digital Systems” that is part of the EuroTraining catalogue and that is held twice per year at the italian site (i.e., COREP, Torino) of EuroTraining.

Concerning internal exploitation, Politecnico di Torino will benefit from its own research carried out within the POET project, as well as from that performed by the other partners (both research institutes and industries), to consolidate its know-how and expertise on high-level low power design methodologies. Politecnico di Torino holds a leading position world-wide in this specific area, as demonstrated by the scientific production of its faculty and affiliated researchers, as well as the number of cooperations and technical consulting it is currently undertaking. Among the companies that are, at this point in time, carrying out joint research with Politecnico di Torino, there are most of the major players of the semiconductor (i.e., ST Microelectronics, Infineon, Intel, National Semiconductors, Samsung Electronics), system/telecom (i.e., Philips, Siemens ICN, Intracom, Hewlett-Packard, Omnitel, Telecom Italia, Infostrada, CSELT), software (i.e., Microsoft) and EDA (i.e., Synopsys, Cadence) scenarios. The POET project will offer to Politecnico di Torino a unique opportunity for consolidating its relationship with the aforementioned companies, as well as for creating new links and contacts with other important actors of the ICT arena.

9. Workplan

9.1. General Description

The following organisation is a mean to achieve the high-level objectives of the project:

Define a consistent and general methodology for power estimation and optimisation of embedded HW/SW systems.
Improve and implement the necessary tools to enable the developed methodology.
Evaluate the methodology and tools.
Quantify the achievements based on user input.
Enable sustained commercial tool exploitation.

The objectives of the project will be achieved by joining the forces of Europe's leading communication and embedded processor industries with well established research centres for low power design and methodologies. However, the objectives stated are very ambitious and could certainly not be achieved without being able to build on previous results and experiences from an earlier co-operation of the kernel set of partners (OFFIS, CEFRIEL, POLITO, ASEL and ARM). During this earlier project which had been rated very positively by the commission, the reviewers, and the partners themselves, the consortium could not only demonstrate its good co-operation, but also excellent scientific and engineering results. These will be brought into the POET project as background information.

A key role in the consortium will be played by the industrial user partners and technology providers (ASEL and ARM). Both will be in charge of defining requirements, application domains and target platforms as well as testing and providing feedback during prototype tool development from concrete product developments. ARM will also supply the technological information which is necessary to the development of design tools usable in practical environments. Research institutes and a university (OFFIS, CEFRIEL and POLITO) will be in charge of carrying out the basic technological investigation of methods that can be fruitfully implemented as automatic design tools; feasibility and effectiveness of the chosen methodologies will be proven through implementation of prototype tools. Finally, the EDA vendor (OSC) will take care of the exploitation of the project results. POET partners will share their work as described in the sequel.

Even if the market for high-level power estimation tools is just emerging, the main risk for the introduction of a new set of tools is the time-to-market: tools are appearing and it is time to define and reserve a place for new tools. The POET project tries to address this issue with a schedule of deliverables that allows at least prototypes of tools to be available quite early during the project, targeting demonstration at the exhibitions of DAC (held annually in the US around mid-June), DATE (held annually during March, in France or Germany), and ASP-DAC held annually in Japan..

If the introduction for new power optimisation tools on the EDA market appears difficult, the consortium may consider an alternative for the exploitation of the tools and methodologies resulting from POET: to provide building-blocks for other CAD companies. Power estimation and optimisation at the high levels of abstraction is becoming an increasingly important design task and system designers are awaiting solutions. Covering this market segment should be of interest for established EDA companies as well.

The workplan is structured into eight Workpackages (WP): six technical, one commercial, and one administrative. Fig. 2 in Chapter 9.6 shows the general structure of the project:

WP1 defines the design flows at the user partners (ASEL and ARM) into which the estimation and optimisation tools will be integrated. The interfaces and required features of the tools are specified in this workpackage. WP1 will be lead by ARM.

WP 2, lead by CEFRIEL, develops methodologies to optimise power consumption of the software parts of Systems on Chip (SoC). It will be based on the power estimation techniques previously developed and enhanced in WP5 and will be dependent on the architecture adopted in terms of processor and memory hierarchy and on the compilation and operating

system environment. Information on the power consumption of the memory will be obtained by the hardware estimators developed by the partners OFFIS and POLITO. ARM will contribute to this workpackage by developing models for the influence of different cache architectures on the power consumption.

WP3 deals with the development of methodologies and a prototype tool for interconnect and data manipulation, transfer and storage driven power optimisation of executable specifications of hardware units including memory structures written in C/C++. This workpackage will be lead and mainly performed by OFFIS.

The development of methodologies and prototype tools for power optimisation of the memory sub-system, of the memory-processor and data-path communication interfaces and, for automatic insertion of power management circuitry in cycle-accurate RTL descriptions will be the thematic contents of WP4 which is lead by POLITO.

WP5 enhances the capabilities of the power estimation tools developed by OFFIS, CEFRIEL and POLITO as part of a previous ESPRIT project in order to make them suitable to interact with the optimisation tools that will be developed in WPs 2, 3 and 4.

WP6 covers the integration of all optimisation and estimation prototype tools into the design flows of the user partners. The evaluation of the estimators and optimisers is also performed by the users in this workpackage. This workpackage is lead by ASEL, however, ARM will also participate in this WP at a similar level of effort.

The exploitation of the results, covered by WP 7, will be twofold:
Internally, results will be exploited by all industrial partners and by the research institutes. This will involve applying the methodology, libraries and tools for future product development, as well as commercial exploitation of the test cases.
Commercial marketing of the tool set by OSC.

Finally the project co-ordination, conflict resolution, administrative handling, and contacts to the EU will be part of WP 8, lead by OFFIS.

9.2. Workpackage List

Work-package No.	Workpackage Title	Lead contractor	Person-months	Start month	End month	Deliverable No
WP 1	Design Flow and Tool Specification	ARM	18	M0	M18	D1.1.1-D1.2.2
WP 2	Software Power Optimisation	CEFRIEL	64	M3	M34	D2.1.1-D2.4.2
WP 3	Algorithm-Level Power Optimisation	OFFIS	54	M3	M30	D3.1.1-D3.3.3
WP 4	Cycle-Accurate RTL Power Optimisation	POLITO	68	M3	M30	D4.1.1-D4.3.3
WP 5	Enhanced Power Estimation Tool Suite	OFFIS	103	M0	M30	D5.1.1-D5.3.4
WP 6	Tool Integration and Evaluation	ASEL	103	M18	M36	D6.1.1-D6.2.4
WP 7	Exploitation and Dissemination	OSC	97	M0	M36	D7.1.1-D7.3.2
WP 8	Project Management	OFFIS	17	M0	M36	D8.1.1-D8.3.6
	Total		524			

9.3. Workpackage Descriptions

9.3.1. Workpackage 1: Design Flow and Tools Specification

9.3.1.1. Introduction

One of the main targets of the POET project is the development of tools that can gain industrial acceptance and can be exploited in the market. This will only be achieved, if the tools to be developed in the project can easily be integrated into mainstream industrial environments and current embedded system design flows. Furthermore the tools must meet the estimation accuracy, optimisation quality, and performance and interface requirements of the users. The experience of the industrial user partners ARM and ASEL has shown, that EDA tools that on the one hand satisfied their feature and performance requirements will certainly not be used, if on the other hand they are not easily integratable into their design flows and vive versa. Hence it is not sufficient to develop high quality tools with just excellent features. A prerequisite to succeed in the market is to meet a common set of industrial requirements.

In order to achieve this target, the industrial user partners ARM and ASEL will provide the tool developers with information on their current design flows and will specify their tool requirements with respect to the issues mentioned above in the beginning of the project. These specifications will be the basis for the tool development and shall guarantee that the tools can be easily integrated into the users design flow and satisfy the industrial needs.

9.3.1.2. Objectives

The objective of this workpackage is the definition of the POET design flow for power estimation and optimisation and the specification of the tool requirements by the user partners ARM and ASEL.

9.3.1.3. Description of work

Workpackage 1 consists of two tasks that are performed by the user partners ARM and ASEL of the project. The task are:

T1.1 Specification of the design flow and
T1.2 Specification of the tool requirements.

The purpose of task T1.1 is to provide the tool developers with information on the current design flows of the industrial partners. This will be a description of the complete design flow and the methodologies and tools that are used for up to date System on Chip designs. In particular these are the methodologies and tools that are used for:

specification and modelling of embedded systems
embedded software design
ASIC design and
hardware/software co-design and co-simulation.

This description will help the developers to implement the tools according to the industrial needs and code of practice and will allow an easier integration of the tools in the design flow of the users.

The aim of task T1.2 is the specification of the tool requirements by the industrial partners. The user requirements shall be specified for

the estimation accuracy and speed of the tools
optimisation potential to be explored
the user interface
supported versions and interfaces of third party tools and
other environmental requirements (operating system, memory, network etc.)

As the requirements of the users concerning e.g. third party tools may change during the project, the users shall provide a refined version of their requirement specification in the middle of the project. The tool development shall rely on the given specification in order to fulfil the industrial needs and thereby allow a successful exploitation of the tools.

9.3.1.4. Major Milestones

M3: Specification of Designflow
M18: Refined Specification of Tool Requirements

9.3.1.5. Duration and effort

Workpackage number:	1		Start date or starting event		M0	
Participant number:	OFFIS	CEFRIEL	POLITO	ASEL	ARM	OSC
Person months per participant:	0	0	0	12	6	0

9.3.1.6. Deliverables

Del. No.	Deliverable name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
D1.1	Specification of Design flow	1	ARM	REPORT	INT	M3
D1.2.1	Initial Specification of Tool Requirements	1	ARM	REPORT	INT	M6
D1.2.2	Refined Specification of Tool Requirements	1	ARM	REPORT	INT	M18

9.3.2. Workpackage 2: Software Power Optimisation

9.3.2.1. Introduction

The goal of this workpackage is to face the problem of power optimisation of the software components of embedded SoCs. In particular the effort will be focused on source-level analysis and optimisation, by using established compilation environments and/or proprietary compilation environments. Since most of the software for embedded applications is developed using C and since all object-oriented extensions to this language lead to a loss of efficiency and an increase in energy requirements, the methodology will concentrate on the ANSI C language. Extensions and libraries compliant with the POSIX standard will also be considered.

The first part of the project will be devoted to the study of the potential sources of power dissipation (memories, CPU internals, etc.) and their relation with the basic C operators and constructs. In order to define a strategy to tackle energy optimisation issues, a detailed analysis of the compilation techniques and environments will be considered as a necessary prerequisite. Furthermore, in order to adequately consider technology specific issues, accurate data concerning the power consumption of ARM cores, cache memories and any other additional components are a necessary and mandatory prerequisite.

Once the relations among power dissipation sources, source code constructs and compilation techniques have been clarified, the work will address the identification of a set of general optimisation directives as independent from the target microprocessor architecture as possible. Technology specific issues will also be addressed and integrated in the general methodology.

The following step consists in the application of the identified directives on a set of benchmarks in order to validate the effectiveness of each source code transformation. Code transformations will be preliminary applied manually. This phase precedes the definition and the implementation of a tool for the semi-automatic application of the identified source-to-source code optimisations.

The implementation of the cache architecture and operation can have a substantial impact on the overall system power consumption – cache size and depth and hit/miss rates, write-buffering type and fetch block size, and cache-flushing decisions all impact the overall system power consumption, silicon area and performance to a considerable degree. In fact, non-optimal cache design can impact both performance and power consumption to a much greater degree than non-optimised core processor design alone.

9.3.2.2. Objectives

The foremost outcomes of this workpackage will be on one hand, a consolidated expertise in the field of software power estimation, and, on the other hand, a methodology and a set of style guidelines for C coding. The methodology will be supported by a complete set of prototype tools. The power optimisation toolset will strongly rely and cooperate with the power estimation toolset developed in WP5, Task 1. The POET tools will be used to optimise the design rules for cache architectures to achieve the best balance between the different requirements specified for the system.

9.3.2.3. Description of work

Task 2.1 concentrates on the identification and modelling of the power dissipation sources in the target platform and their relations with the basic C operators and constructs. The understanding of such relations will enable the definition of source-to-source transformations

(Task 2.3) aimed at the reduction of the overall power budget of software programs. A prototype toolset for code analysis will be delivered at the end of the task. The toolset will mostly provide timing/power analysis and interfacing capabilities. The toolset will also implement a preliminary front-end for the semi-automatic power code transformation routines.

Task 2.2 is based on the expertise and data harvested in Task 2.1, the analysis will be extended to library components. New problems, mostly regarding the unavailability of source code of third-party libraries, will be tackled relying on the theoretical models and software tools developed in Task 2.1.

Task 2.3 will provide a structured set of design and coding guidelines aimed at delivering a power-aware software development methodology. In a successive phase some of the guidelines will be considered for automatic or semi-automatic implementation. In particular the tool will provide two distinct features: on one side the analysis of the source code aiming at identifying power-critical sections and sections/constructs eligible for source-to-source code transformations; on the other side a prototype set of routines for semi-automated application of the identified transformations will be implemented.

In Task 2.4 ARM will apply the POET tools and methodology to the design characterisation of SoC designs which include an on-chip cache-based processor (as is typically found in most such designs). The POET approach will be used to synthesise real applications with varying elements of cache architecture and implementation, to characterise the consequences for power consumption and performance in each instance.

9.3.2.4. Major Milestones

M18: Prototype tool for source code analysis and front-end for code transformations of basic C constructs
M18: Preliminary Models for the Influence of cache architectures on power dissipation
M30: Prototype tool for power optimisation of C source code
M34: Power models of cache architectures for embedded microprocessors

9.3.2.5. Duration and effort

Workpackage number:	2		Start date or starting event		M3	
Participant number:	OFFIS	CEFRIEL	POLITO	ASEL	ARM	OSC
Person months per participant:	0	36	0	0	28	0

9.3.2.6. Results

Res. No.	Result name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
R2.1	Prototype for power optimisation for basic C-constructs	2	CEFRIEL	PROTOTYPE	INT	M18
R2.4	Prelim. models for influence of cache architecture on power	2	ARM	REPORT	INT	M18

9.3.2.7. Deliverables

Del. No.	Deliverable name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
D2.1	Identification of main power effects related to memory management and processor architecture and related techniques for power reduction	2	CEFRIEL	REPORT	INT	M12

D2.2	Power reduction related to library and operating system calls and design guidelines at source code level	2	CEFRIEL	REPORT	INT	M24
D2.3.1	Prototype version of a tool for power optimisation of C source code	2	CEFRIEL	PROTOTYPE	PUB	M30
D2.3.2	Bug fixing and final user manuals	2	CEFRIEL	REPORT	PUB	M34
D2.4	Power models of cache architectures for embedded microprocessors	2	ARM	REPORT	INT	M34

9.3.3. Workpackage 3: Algorithmic-Level Power Optimisation

9.3.3.1. Introduction

New methodologies for power optimisation of the hardware part of embedded systems at the algorithm level are developed and implemented in this workpackage which is divided into three tasks T3.1 to T3.3. These new techniques will be integrated into the high-level power estimator ORINOCO®. ORINOCO® has been developed in the ESPRIT project PEOPLE. The tool allows a power aware design space exploration starting from behavioural VHDL descriptions. The impact of binding and allocation of hardware resources on the power consumption is estimated. Investigations of several benchmarks has revealed that binding and allocation have a large impact on the power consumption. This is because these two synthesis steps define the data streams which are processed by the hardware units. Being a limitation, a fixed schedule is generated in the current version of the tool.

ORINOCO® estimates a lower and an upper bound on the power consumption due to the possible large spread in power consumption of the innumerable hardware architectures which can be synthesised from a behavioural specification. Heuristics are already implemented which compute from the estimated lower bounds near optimal allocations and bindings for the individual hardware resources. These implementations will form the basis for the developments in this workpackage.

Two different kinds of optimisations are addressed: Support for low power high-level synthesis (T3.1) and low power algorithm transformations (T3.2 and T3.3). The latter produces the input for the first one in the design flow. Low power algorithm transformations modify a given algorithmic hardware description such that the required energy to execute the algorithm in hardware is reduced. The function computed by the algorithm is kept unchanged. A lot of approaches have been published in the literature which address these types of optimisations to increase performance or reduce the energy requirements. However, none of these approaches considers all aspects of the power cost function during the optimisation. In particular, the interconnect costs becoming the dominating factor for SoCs is generally not taken into account. The methodologies and tools which will be developed in this workpackage will consider all aspects of the cost function. The power costs will be computed with the available algorithm power estimator to be enhanced in workpackage 5 (T5.2).

Support for low power high-level synthesis means to help the designer in making decisions. It is not intended to develop a high-level synthesis tool from scratch because writing a new synthesis tool would take too much man power. Synthesis of interfaces and appropriate control logic as well as supporting large and flexible libraries are very complex tasks. Good high-level synthesis tools like the Behavioural Compiler® from Synopsys are already on the market. Instead of writing a new tool, the designer will be aided during the synthesis of the design by hand or with commercial tools.

The supported design description language will be C/C++ with a focus on the SystemC semantic definitions. ORINOCO® has already a prototype of a language interface for imperative C descriptions. This interface will be completed to handle the full C++ standard and extended to extract the semantics of SystemC in T5.2 of workpackage 5.

Possible candidates for low power algorithm transformations are based on the commutative, associative and distributive laws of arithmetic and loop transformations to reduce for example the storage costs by restructuring array accesses. The transformations have to be carried out in such a way that the following high-level synthesis step can take advantage of spatial and

temporal locality in the input description. Spatial locality is a prerequisite for reduced interconnect cost while temporal locality minimises storage access costs.
The most important sub-tasks which will be addressed are scheduling, binding and allocation of arithmetic and storage access operations for low power taking interconnect effects into account.

9.3.3.2. Objectives

The objective of this workpackage is to extend ORINOCO® to support low power high-level synthesis and automatic algorithm transformations. These power optimisation capabilities are performed on hardware specifications written in SystemC. The unique feature of these optimisations is that all power cost contributors are considered.

9.3.3.3. Description of work

In this workpackage, OFFIS will extend the available high-level power estimator ORINOCO® with optimisation capabilities. The workpackage is divided into three distinct tasks.

Task 3.1 deals with low power high-level synthesis. The tool will output synthesis constraints which minimise the total power consumption of hardware blocks covering functional units, interconnects and steering logic, control logic as well as memories. Different optimisation heuristics will be evaluated. The starting point of the heuristics will be the binding and allocation solutions for the individual hardware resources which can be already computed with ORINOCO®. A low power scheduler will be added to the tool. The scheduler has to identify which operations should not be executed in parallel to allow low power resource sharing. Timing constraints have to be taken into account. The new heuristics have to find a global low power solution taking all power contributors into account. The output of this optimisation step are high-level synthesis constraints. An interface to the Synopsys CoCentric SystemC Compiler will be made available.

In Task 3.2, a methodology and a prototype implementation will be developed which outputs transformations of an executable specification in C/C++ such that the power consumption of the arithmetic is minimised taking the interconnections and the switching activity on them into account. This task focuses on the datapath of the design. Possible candidates for low power algorithm transformations are based on the commutative, associative and distributive laws of arithmetic. Loop transformations are another way to rewrite a given specification. The task will identify what kind of transformations are the most promising ones and in which order they should be executed. Heuristics will be developed which evaluate the candidate transformations in a tight loop using the high-level power estimator and optimiser of Task 3.1. Task 3.2 also includes the data storage and retrieval operations in the optimisation phase. Accesses to arrays which will result in memory accesses are transformed such that the total power consumption of the memory structure as well as of the buses is minimised. The transformations have to be carried out in such a way that the following high-level synthesis step can take advantage of spatial and temporal locality in the input description. Spatial locality is a prerequisite for reduced interconnect cost while temporal locality minimises storage access costs.

9.3.3.4. Major Milestones

M24: final version of the tool to support low power high-level synthesis.
M30: final version of the tool which performs low power specification transformations.

9.3.3.5. Duration and effort

Workpackage number:	3		Start date or starting event		M3	
Participant number:	OFFIS	CEFRIEL	POLITO	ASEL	ARM	OSC
Person months per participant:	54	0	0	0	0	0

9.3.3.6. Results

Res. No.	Result name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
R3.1.1	Interconnect driven low power high-level synthesis	3	OFFIS	REPORT	INT	M9
R3.1.2	Tool for supporting low power high-level synthesis (prelim.)	3	OFFIS	PROTOTYPE	INT	M12
R3.2	Tool for source code transformations (data path power) (prelim.)	3	OFFIS	PROTOTYPE	INT	M18
R3.3	Tool for source code transformations (memory power) (prelim.)	3	OFFIS	PROTOTYPE	INT	M18

9.3.3.7. Deliverables

Del. No.	Deliverable name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
D3.1	Tool for supporting low power high-level synthesis (final)	3	OFFIS	PROTOTYPE	PUB	M24
D3.2.1	Source transformations to minimise memory and data path power	3	OFFIS	REPORT	INT	M15
D3.2.2	Tool for source code transformations (memory and data path power)	3	OFFIS	PROTOTYPE	PUB	M30

9.3.4. Workpackage 4: Cycle-Accurate RTL Power Optimisation

9.3.4.1. Introduction

In spite of the recent effort made by the research community to raise the level of abstraction at which the design process starts, RTL is still the description style used by most designers involved in the development of digital systems.

Due to the scaling of electronic technologies, design tools currently available are rapidly becoming obsolete; EDA suppliers are thus requested to provide the design community with new generations of tools which are able to cope with the increased complexity and tighter constraints that must be faced when carrying out the design of deep-submicron circuits and systems.

Although some effort has already been made by EDA vendors in the area of RTL power optimisation, available solutions are just preliminary and far from being satisfactory. Substantial research and development work is therefore required in order to make the EDA technology for RTL low-power design competitive and usable with confidence in practical design settings

9.3.4.2. Objectives

Objective of WP4 is the development of methodologies and prototype tools for the optimisation of power consumption of a cycle-accurate, RTL description. Power reductions will be achieved through different architectural techniques, that can be categorized into three classes:

Memory hierarchy optimisation;
bus interface optimisation;
dynamic power management.

These three classes are addressed in the corresponding tasks T4.1 to T4.3. According to the (recent) scientific literature, some techniques in the classes above have shown very good potential, when applied (by hand and not in a fully worked-out manner) to some benchmark examples. Purpose of this workpackage is thus two-fold: First, to investigate innovations to, and improvements of the currently available technology for RTL power optimisation. Second, to make the newly developed methods and corresponding prototype tools applicable in practice to real-life applications, such as those provided by the user partners of the consortium. This with the target of setting up the stage for the creation of an industry-strength RTL power optimisation flow that will be eventually exploited by OSC, the EDA vendor of the POET consortium, and its subcontractor BullDAST.

Enabling technology for the development and usage of the cycle-accurate RTL power optimiser will be the RTL power estimator developed by POLITO in the context of the ESPRIT project PEOPLE, whose capabilities will be enhanced and adapted to the optimisation flow as part of workpackage 5 (Task T5.3).

9.3.4.3. Description of work

In Task 4.1, we will develop a methodology and a prototype tool for the design of a low power memory sub-system, which embodies generation of the memory architecture (i.e., caches, buffers, partitioned SRAM/DRAM/FLASH) and of the corresponding control and management logic. Driving criterion for the optimisation will be the locality of memory accesses to low power memory banks of different nature. Technology factors such as bus and control logic layout will also be taken into account during memory hierarchy generation.

In Task 4.2, we will develop a methodology and a prototype tool for power optimisation of communication interfaces (i.e., memory and data-path buses). This will imply the development of bus encoding techniques for low power data transfer. Both general-purpose (e.g., adaptive) and special-purpose (profile-driven) schemes will be supported. Bus interface optimisation will target reductions of the switched capacitance associated to communication channels; in particular, the focus will be on techniques that minimize bus activity under realistic (i.e., layout-linked) bus models; pure functional optimisation (i.e., number of logic transitions) is, in fact, no longer meaningful for current, sub-micron technologies, and new schemes (both adaptive and profile-driven) will be investigated. Issues related to automatic synthesis of the interface logic, as well as verifiability of the encoded communication channels, will also be considered.

In Task 4.3, we will develop a methodology for the automatic insertion into the synthesisable part of the RTL description of the logic that controls different types of power management circuitry. Dynamic power management approaches that will be developed will span a large variety of solutions, ranging from architectural techniques (e.g., operand guarding, pre-computation, clock and enable management) to functional and simulation-based techniques (e.g., extraction of computational kernels, block decomposition), thus providing a suite of methods that could be applied to a large number of different situations and under different design and operation circumstances.

9.3.4.4. Major Milestones

M30: Final version of the tool for low power memory and communication interface design and for dynamic power management

9.3.4.5. Duration and effort

Workpackage number:	4		Start date or starting event		M3	
Participant number:	OFFIS	CEFRIEL	POLITO	ASEL	ARM	OSC
Person months per participant:	0	0	60+8	0	0	0

9.3.4.6. Results

Res. No.	Result name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
R4.1	Tool for low-power memory and communication interface design and for dynamic power management (prelim.).	4	POLITO	PROTOTYPE	INT	M18

9.3.4.7. Deliverables

Del. No.	Deliverable name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
D4.1	Techniques for low-power memory and communication interface design and for dynamic power management.	4	POLITO	REPORT	INT	M12
D4.2	Tool for low-power memory and communication interface design and for dynamic power management (final).	4	POLITO	PROTOTYPE	INT	M30

9.3.5. Workpackage 5: Software, Algorithm and RTL Estimators

9.3.5.1. Introduction

In workpackage 5, the prototype power estimators which were developed in the previous ESPRIT project PEOPLE are enhanced to make them suitable to interact with the optimisation tools developed in WP 2, 3 and 4 (T5.1 to T5.3 respectively). Three prototype estimators addressing the embedded software as well as the hardware at the algorithm and structural RT level are available.

The software estimation toolset for the C language to be enhanced in T5.1 consist of two components: the high-level estimation tool, operating on the C sources, and the low-level estimation tool operating on the compiled assembly code. A software application is considered as a collection of functions, in the sense that the tool provides accurate estimations at the granularity of the function. More fine-grained figured can also be obtained but their accuracy is strongly dependent on the level of optimisation used when compiling. The source-level estimation tool parses one source file at a time and generates the corresponding static estimates. To this purpose no other tools are necessary and in particular the code need neither to be compiled nor executed. To obtain a dynamic estimate, the code must be compiled, linked and run on a generic host machine, not necessarily the same machine it has been designed for. All data necessary to perform the estimation are collected into processor-dependent library files. The assembly-level estimation tool operates on the complete assembly code of the software under investigation. The user can select specific portion of the code for the analysis, rather than the complete code. This option significantly speeds up the estimation process. To obtain static estimates for a given machine a compiler for that processor is necessary. Since the code does not need to be executed, a cross-compiler might also be used. For dynamic estimation the code needs either to be run on the target processor or to be simulated with a suitable (third-party) instruction set simulator.

An ANSI C/C++ front-end will be added to the existing algorithm power estimator ORINOCO® which has a VHDL front-end and an interface for a subset of imperative C at the moment (T5.2). C/C++ descriptions are more common at the algorithm specification level. This language extension will make it possible to address a larger market segment. Internally, the estimation kernel of the tool is independent from the input language which allows a transition to different languages. The front-end will be designed for the semantics of SystemC. The estimation kernel itself will also be enhanced in this workpackage. Investigations have shown that lower level issues like unnecessary switching activity or logic optimisations by the synthesis tool can have a large impact on the power consumption and should hence be considered in the estimation. The availability of a fast yet accurate estimation kernel is crucial for the algorithm optimisation tasks of workpackage 3.

Concerning cycle-accurate, RTL power estimation, the objectives that will be pursued within this workpackage are related to the enhancement of the capabilities of an existing prototype tool which handles purely structural VHDL, while it is not able to deal with descriptions containing behavioural constructs (T5.3). An additional shortcoming of the tool in its actual stage is that power due to possible glitches that may occur on the connections between macro-blocks is not properly included in the total estimated power. On the other hand, the estimator is based on a technologically-advanced strategy for automatic characterisation and construction of power macro-models and on a cache-based mechanism for model re-use that enables the calculation of very accurate power estimates in a time which is usually a fraction of the running time of state-of-the-art RTL power estimators nowadays available on the EDA market. Enhancing the tool with cycle-accurate estimation capabilities and with the ability to handle the dynamic component of power, as planned in the activities of this workpackage, will thus produce two main benefits: First, it will allow the usage of the tool in the context of the RTL optimisation flow targeted in WP4 of this project. Second, it will simplify the commercial

exploitation of the tool by the EDA vendor partner CR6. RTL estimation tools that merge together flexibility in the input description format with efficient and accurate modelling capabilities are currently not available on the market, while they are seen as a major need by designers from most semiconductor companies and system houses. The exploitation plan for the results of POET is described in more detail in WP7 (section 9.3.7) later in this document.

9.3.5.2. Objectives

The objective of this workpackage is to enhance the capabilities of the available power estimation tools developed as part of the previous ESPRIT project PEOPLE in order to make them suitable to interact with the optimisation tools developed in workpackages 2, 3 and 4.

9.3.5.3. Description of work

In Task 5.1 CEFRIEL will enrich and refine the models adopted for assembly-level and C-level timing and power consumption estimation. In particular delays and power overheads due to pipeline stalls will be analysed and the models will be updated accordingly. Such models will be enhanced by defining a suitable theoretical background in order to account for the aforementioned dynamic effects within the previously defined static estimation techniques. The second part of the Task will be devoted to the implementation of a set of tools automating the static power estimation process.

In Task 5.2, OFFIS will add an ANSI C/C++ language interface to ORINOCO®. The semantics of SystemC will be supported. Adding a new language to the tool implies two things: First, a control/data flow graph has to be extracted from the language. Since the hardware semantics of SystemC are based on templates (specifying bitwidths etc.), C++ templates have to be supported. The second part is the source code instrumentation. The power estimation and hence also the optimisations to be developed, are based on an execution profile of the design specification. The C++ has to be instrumented in order to extract switching information during program execution. This instrumentation has to be performed in an automatic way. Task 5.2 also enhances the estimation kernel of ORINOCO®. The following capabilities will be added: support for timing constraints, pre-computation, clock-gating, unnecessary activity at inputs of functional units during idle cycles, consideration of logic optimisations of units due to unused or constant inputs/outputs. Gate-level effects like unnecessary transitions and the impact of logic synthesis are very hard to predict at the higher levels. The available power models and methodologies have to be extended to deal with these issues.

In Task 5.3, POLITO will enhance the existing (structural) RTL power estimator developed within the PEOPLE project with capabilities for fast, "inner loop" power estimation suited for driving cycle-accurate RTL optimisation. Two kinds of improvements are planned: First, support of behavioural constructs in the input VHDL description to allow cycle-accurate RTL power estimation. Second, support for glitch power estimation capabilities to account for power consumed by the interconnect due to spurious transitions occurring during macro-to-macro signal transmission. A new version of the RTL power estimator that incorporates the new capabilities is the main result that will be achieved in this task.

9.3.5.4. Major Milestones

M12: Prototype Tools for static power estimation
M12: C/C++ and SystemC interface for ORINOCO®
M30: Final version of the tool for cycle-accurate RTL power estimation
M34 Enhanced tool including dynamic estimation and user manual
M30: Enhanced algorithm level power estimation kernel for ORINOCO®)

9.3.5.5. Duration and effort

Workpackage number:	5		Start date or starting event		M0	
Participant number:	OFFIS	CEFRIEL	POLITO	ASEL	ARM	OSC
Person months per participant:	35	22	36+10	0	0	0

9.3.5.6. Results

Res. No.	Result name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
R 5.1	Tool with enhanced software level estimation capabilities (prelim.)	5	CEFRIEL	PROTOTYPE	INT	M18
R5.2	Tool with enhanced algorithm level estimation capabilities: (prelim.)	5	OFFIS	PROTOTYPE	INT	M18
R5.3	Tool for cycle-accurate RTL power estimation capabilities (prelim.)	5	POLITO	PROTOTYPE	INT	M18

9.3.5.7. Deliverables

Del. No.	Deliverable name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
D5.1	Enhanced Tool including dynamic estimations and user manual	5	CEFRIEL	PROTOTYPE	PUB	M30
D5.2.1	Prototype tool with ANSI C/C++ front-end and enhanced behavioural power estimation kernel	5	OFFIS	PROTOTYPE	INT	M12
D5.2.2	Tool with enhanced estimation capabilities: (final)	5	OFFIS	PROTOTYPE	PUB	M30
D5.3.1	Adding cycle-accurate and dynamic capabilities to a structural RTL power estimator	5	POLITO	REPORT	INT	M12
D5.3.2	Tool for cycle-accurate RTL power estimation (final.)	5	POLITO	PROTOTYPE	PUB	M30

9.3.6. Workpackage 6: Tool Integration and Evaluation

9.3.6.1. Introduction

One of the prerequisites for a successful exploitation of the developed tools is their ability to work properly in typical environments of the industry. The tools should be easily integratable into the users design flow and cover all required interfaces to common third party tools in the industry. To fulfil this requirement the industrial partners will describe their design flow, environment and tool requirements in workpackage 1 and the developers will implement the tools accordingly.

After implementation of the tools, they shall be integrated and evaluated at the users site in order to test if they hold the industrial requirements and to further adapt and optimise them corresponding to the users feedback. This will be an interactive process with a tight cooperation between the developers and the users. This tight loop, covering the tool evaluation by users with constant feedback and the tool adaptation and optimisation by the developers shall guarantee that the tools meet the industrial requirements in all respects and allow a successful exploitation of the tools after the project.

9.3.6.2. Objectives

The objective of this workpackage is the integration of all optimisation and estimation prototype tools into the design flow of the user partners and the evaluation of the tools at the users site. The Evaluation will be performed with typical applications from the domains of the user partners ARM and ASEL.

9.3.6.3. Description of work

One of the main efforts that the project will undertake is a field test of the methodology and tool set to evaluate it for real industrial projects. ARM and ASEL will engage in two efforts to evaluate the tools and the design flow in task 6.1 and 6.2.

First prototype tools will be released in the middle of the project and integrated in task T6.1 at the users site of ARM and ASEL. This will require intensive on-site support from the developers, as the design flows of the industrial partners are proprietary and slightly differ from each other with respect to the environments and third party tools that are used.

After successful integration of the tools, they will be evaluated in task T6.2 with first examples from typical applications of the users. During the evaluation phase, the users will constantly provide feedback to the developers, i.e. report bugs and limitations and make suggestions for improvements for the next releases of the tools. In the next step, the developers will adapt and improve the tools according to the users feedback and provide new releases later on. The new releases will again be integrated at the users site and evaluated by the industrial partners. The applications that are used for evaluating the tools are taken from typical System on Chip designs of the users. These include some small examples for testing the prototype tools of the first release as well as whole real life designs examples with typical industrial complexity.

The software prototype implemented by CEFRIEL is a standalone tool, that will not have any integration in a standard design flow. The three person months will be dedicated to installation of the tool on-site.

9.3.6.4. Major Milestones

9.3.6.5. Duration and effort

Workpackage number:	6		Start date or starting event		**M18**	
Participant number:	OFFIS	CEFRIEL	POLITO	ASEL	ARM	OSC
Person months per participant:	10	3	18	36	36	0

9.3.6.6. Results

Res. No.	Result name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
R6.1.1	Integration of algorithm and RT level prototypes (preliminary)	6	OFFIS	REPORT	INT	M21
R6.1.2	Integration of software, algorithm and RT level optimiser prototypes (final)	6	OFFIS	REPORT	INT	M33

9.3.6.7. Deliverables

Del. No.	Deliverable name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
D6.2.1	Preliminary evaluation report issued by ASEL	6	ASEL	REPORT	INT	M24
D6.2.2	Preliminary evaluation report issued by ARM	6	ARM	REPORT	INT	M24
D6.2.3	Final evaluation report issued by ASEL	6	ASEL	REPORT	INT	M36
D6.2.4	Final evaluation report issued by ARM	6	ARM	REPORT	INT	M36

9.3.7. Workpackage 7: Dissemination and Exploitation

9.3.7.1. Introduction

The exploitation of the project results is performed in this workpackage. The first task T7.1 of this workpackage is to update the market analysis already performed by OSC which lead to this POET project proposal. All the partners, according to their specific interests and missions, will participate in the exploitation effort in the tasks T7.2 (dissemination) and T7.3 (exploitation). To assure the external promotion of the tools developed within this project, OSC, in collaboration with the other partners, will take charge of the organisation of tool demonstrations during CAD conferences and exhibitions. This includes the Design Automation Conference (DAC) in the USA, the Design Automation and Test in Europe (DATE) Conference, and the ASP-DAC in Asia. Other promotion actions, such as publications and web advertising, will be undertaken during the project.
In order to strengthen the commercial exploitation possibilities, during the project lifetime joint marketing agreements for the POET tools will be sought with other EDA vendors or distributors.
Demonstrating tool prototypes at international exhibition(s) *during* the project will provide the partners with significant feedback on their tools from potential customers, and thus will help them to take action and improve the tools and reduce the risks of commercial failure. Besides the external promotion during international conferences, OSC will also co-ordinate the definition of the future exploitation plans of all the partners of this project, i.e., for the consortium as a whole, as well as for each individual partner. A draft of these exploitation plans will be delivered at the mid-term of the project; the final exploitation plans will be delivered at the end of the project.

OSC will subcontract to BullDAST some of the work in WP7 for a total of 24 PM, equally distributed over the project lifetime (i.e. 8 PM per year). The costs to be covered by the subcontract are personnel costs (90% of the subcontracted budget) and other specific costs related to the participation to exhibits and fairs of BullDAST (10% of the subcontracted amount). CEFRIEL will subcontract to BullDAST the work in WP7 for a total of 3 PM equally distributed over the project lifetime (i.e. 1 PM per year).

The algorithm level power estimator ORINOCO will cost around 50.000 USD per license. This is the prize for the VHDL as well as the C/C++ version. The estimated license cost for the algorithm level optimizer is around 60.000 USD. The optimiser license includes the estimator. The list of potential customers includes, but it is not limited to: Oticon, Matsushita, Epson, TI, and Infineon.

The estimated cost per license for the stand-alone version of the RTL power estimator will be around 10.000 USD; on the other hand, the cost for the license of the RTL power optimizer, which will only be available together with the RTL estimator, will be around 18.000 USD. Reduced/discounted rates will be made available for trial versions of the software, as well as for companies which already hold a business relation with BullDAST. Finally, special promotions for academic institutions or non-profit research centers will be provided. The list of potential customers includes, but it is not limited to: STM, Intracom, Infineon, Philips, Intel, National Semiconductors and Samsung Electronics of Korea.

To get a closer involvement of Nokia and Siemens first contacts to Nokia have been established by OFFIS. The first prototypes of the POET tools will be presented at Nokia, Finland and possibly other Nokia sites. Evaluation licenses will be provided to them. Their feedback regarding tool enhancements will be considered in the development. Siemens was a project partner of the PEOPLE project. Siemens is already familiar with the PEOPLE tools which will form the basis for the POET developments. They also will get evaluation licenses and their comments will be considered.

9.3.7.2. Objectives

The objective of this workpackage is the preparation of the exploitation and dissemination of the project results. Promotion of the tools will be performed at various exhibits. The goal is to create awareness of the tools in European system houses and to bring continuous feedback from potential customers into the consortium.

9.3.7.3. Description of work

OSC will adopt the following exploitation strategy for the tools developed within the POET project:

Promote the tool prototypes and their advanced techniques at various trade shows.

Utilise existing and develop new channels into the European communications industry to make them aware of the functionality, efficiency and gain of the tools.

Based on the industrial feedback, as well as on the user partners' experiments, adapt the tools accordingly and promote beta-evaluations by potential customers inside and outside the consortium.
Based on the results of these beta-evaluations and the interests shown, make a decision regarding further investment, in order to make products from the project tool prototypes.

If products have been released and several customers found, investigate and identify distribution channels to market the tools world wide.

Each of the steps above is conditioned by the success of its preceding step and is described in the following sections.

Promotion of prototypes at various exhibits

Starting with the tool prototypes of the PEOPLE project OSC will organise demonstrations of the tools at various exhibitions and conferences. In contrast to less application focussed tools, OSC will concentrate its efforts during the earlier phases of the exploitation on the European market, extend it later to the Japanese market and finally address the US market. Hence primary events of demonstrating the POET tools will be the Design Automation and Test in Europe (DATE) Conference and Exhibition, and the Asian-Pacific DAC, (ASP-DAC) conference and exhibition. OSC will be present at the annual Design Automation Conference (DAC) in the US, because this is the largest event of its kind worldwide with even many Europeans and Japanese attending. Further DAC offers opportunities to create interest of potential customers. OSC will invite the tool developers to join these events and collaborate in the presentation of the tools as well as to be available for their technical expertise and knowledge of the prototypes. The budget of 150.000 € (column "other significant project costs" in the financial forms) is calculated for annual visits of the DAC and DATE and the estimate of the costs is based on experiences of partners from other projects.

Demos at potential customer sites

In order to increase visibility of the project results, and thus increase the chances for tool marketing, OSC (and its subcontractor BullDAST) will demonstrate the POET prototypes directly at the sites of potential customers. Concerning the marketing of ORINOCO, OSC will give presentations of the tool at the beginning of the project for potential customers to which OFFIS has already established contacts. These companies are: Oticon, Matsushita, Epson, TI, and Infineon. Hopefully, new companies can be attracted at exhibitions like DAC or DATE.

On the other hand, BullDAST will demonstrate the RTL estimation and optimization tools to semiconductor industries and system houses with whom some partnership or business agreement does exist, namely ST Microelectronics, Infineon, Philips, Siemens, Intracom, Intel (in the USA), Samsung Electronics (in Korea) and National Semiconductors (in the USA).

Create awareness in European system houses

Building on existing leads into major European system houses and exploiting further channels to the Design Technology Groups of leading communication industries OSC will disseminate the information about the application, the efficiency and the possible gain into industry. It is the objective of this task to further refine the requirements for the POET tools, to adapt them to changes in the market and the demand as well as to position them strategically.

The possible result of this effort will be :

Beta evaluations by various potential customers

The next step is to gain the interest of potential customers outside the consortium in evaluating the POET tools and techniques. It is important to understand that the timing of these evaluations has to be chosen very carefully in order to achieve positive effects and to reduce the effort required to support such beta evaluations. OSC has experience in supporting tool evaluations of our verification tools. In order to conduct the evaluations with sound technical experience, OSC has to rely on the active support of the tool builders Politecnico di Torino, CEFRIEL and OFFIS. In the case the SW- and the RT-Level optimiser the evaluations will be closely accompanied by the subcontractor BullDAST.

Product industrialisation

Once several potential customers have shown a real interest in the acquisition of the tools, investments must be made by OSC to industrialise the prototypes and market the resulting products. For the algorithmic estimator and optimiser, the industrialisation will include a technology transfer (transfer of the know-how) from the research partner OFFIS to the EDA partner OSC. The transfer of the source code will be prepared up-front by having OFFIS and OSC agree on coding guidelines at the start of the project’s programming phase. The industrialisation of the RT-Level estimator and optimiser will be done by BullDAST. BullDAST will continue to be responsible for the support, maintenance and further development of these tools.

BullDAST will also promote and exploit the SW power estimator and optimiser developed by CEFRIEL. Since the marketing opportunities for EDA tools addressing SW estimation/optimisation are still not fully explored, and since the SW estimation/optimisation prototypes developed in POET will be inevitably targeted towards specific software development kits (e.g., the gcc compiler), tool industrialisation will be carried out by CEFRIEL/BullDAST at later stages. Promotion and dissemination, as well as market investigation (i.e. distribution of evaluation copies) for the SW estimation and optimisation tools will be done by BullDAST using CEFRIEL's prototypes, instead of the reengineered versions. However, if a tool engineering phase will be required in order to increase the marketing opportunities of the tools, an agreement will be established between CEFRIEL and BullDAST with the purpose of carrying out this additional piece of work.

OSC and BullDAST will agree on a joint marketing contract of the different tools of the POET tool set. This is to utilise the existing leads into industry of both companies, synergy in setting up a marketing infrastructure while concentrating their technical skills on those parts of the tool suite which have been developed by the respective local research partners.

World-wide distribution channels

OSC has been founded in 1999. It currently employs 21 engineers. According to the predicted growth rate, OSC is going to have some 30 employees by the end of 2001. OSC has been profitable from the first day. Still an EDA vendor of this size, cannot market end-user EDA products alone. The experience with our formal verification tools shows that joint marketing agreements allows to reduce the own effort for marketing and concentrate on the technical consolidation, the development of new features and the support, training and consultation.

Hence OSC will only address key accounts in Europe directly. In order to cope with the limited resources available during the start-up phase, the focus will be on a small number of large industries in the beginning. The expectation is that the amount of support per license is lower than in SMEs.
In the medium term, however, also SMEs shall benefit from the POET tools. For them a more mature status is needed to reduce their own and the OSC support effort. Since it is not in the current business line of OSC to set up a major marketing organisation of its own, the co-operation with distribution channels will be sought.

In the long term the marketing of such tools is always world-wide (Europe, United States and Far-East) and requires local support for pre-sale and post-sale activities. While OSC only handles direct marketing to major key accounts within Europe, it will require collaboration to address the American and Asian markets. OSC will hence seek to establish several distribution channels for its end-user products. The Japanese market is the second largest EDA market world wide. The Japanese - like the Europeans - have a focus on signal processing, however, more in consumer products than in telecom. Despite the fact that there is no major local EDA industry in Japan, the Japanese industry traditionally is more open to non-mainstream EDA solutions than the US industry (and unfortunately the European industry). Hence after the European, we will first address the Japanese market through local agents and/or DA integrator companies which are successfully working in the Japanese market. Major EDA exhibitions and trade shows will be used to seek the contact to these distributors. Existing contacts to Japanese industry and academia will be used to select the most reliable and promising partners.

9.3.7.4. Major Milestones

9.3.7.5. Duration and effort

Workpackage number:	7		Start date or starting event		M0	
Participant number:	OFFIS	CEFRIEL	POLITO	ASEL	ARM	OSC
Person months per participant:	6	0+3	9	2	2	51+24

9.3.7.6. Results

Res. No.	Result name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
R7.1.1	Market overview	7	OSC	REPORT	PUB	M6

9.3.7.7. Deliverables

Del. No.	Deliverable name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
D7.2.1	Draft Exploitation Plan	7	OSC	REPORT	INT	M12
D7.2.2	Final Exploitation Plan	7	OSC	REPORT	INT	M36

9.3.8. Workpackage 8: Project Management

9.3.8.1. Introduction

The Project Management is described in 9.7.

9.3.8.2. Objectives

The objective of this Workpackage is the management of the project according to the procedures described in section 9.7.

9.3.8.3. Description of work

The main tasks to be performed by the management are: co-ordination of work, cost control, reporting, conflict resolution, progress monitoring, contingency plans and follow-up procedures.

9.3.8.4. Major Milestones

The Major milestones are the Cost statements every 12 months and the Periodic Management reports every 3 months

9.3.8.5. Duration and effort

Workpackage number:	8		Start date or starting event		M0	
Participant number:	OFFIS	CEFRIEL	POLITO	ASEL	ARM	OSC
Person months per participant:	3	2	3	3	3	3

9.3.8.6. Deliverables

Del. No.	Deliverable name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
D8.1.1	Project Consortium Agreement	8	OFFIS	REPORT	INT	M3
D8.2.1-D8.2.3	Periodic Progress Reports (every 12 months)	8	OFFIS	REPORT	INT	M12-M36
D8.3.1-D8.3.12	Periodic Management Reports (every 3 months)	8	OFFIS	REPORT	INT	M3-M36
D8.4.1-D8.4.3	Cost statements (every 12 months)	8	OFFIS	REPORT	INT	M12-M36

9.4. Effort Overview

9.4.1. Effort per WP (total)

Work-package No.	Workpackage Title	Lead contractor	Start month	End month	Person months
WP 1	Design Flow and Tool Specification	ARM	M0	M18	18
WP 2	Software Power Optimisation	CEFRIEL	M3	M34	64
WP 3	Algorithm-Level Power Optimisation	OFFIS	M3	M30	54
WP 4	Cycle-Accurate RTL Power Optimisation	POLITO	M3	M30	68
WP 5	Enhanced Power Estimation Tool Suite	OFFIS	M0	M30	103
WP 6	Tool Integration and Evaluation	ASEL	M18	M36	103
WP 7	Exploitation and Dissemination	OSC	M0	M36	97
WP 8	Project Management	OFFIS	M0	M36	17
Subtotal					524
	Coordination	OFFIS			18
Total					542

9.4.2. Effort per WP (per partner)

Workpackage No.	OFFIS	CEFRIEL	POLITO	ASEL	ARM	OSC	Total
WP 1	0	0	0	12	6	0	18
WP 2	0	36	0	0	28	0	64
WP 3	54	0	0	0	0	0	54
WP 4	0	0	68	0	0	0	68
WP 5	35	22	46	0	0	0	103
WP 6	10	3	18	36	36	0	103
WP 7	6	3	9	2	2	75	97
WP 8	3	2	3	3	3	3	17
Subtotal	108	66	144	53	75	78	524
Coordination	18	0	0	0	0	0	18
Total	126	66	144	53	75	78	542

9.5. List of Results (distributed inside the consortium)

Res. No.	Result name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
R2.1	Prototype for power optimisation for basic C-constructs	2	CEFRIEL	PROTOTYPE	INT	M18
R2.4	Prelim. models for influence of cache architecture on power	2	ARM	REPORT	INT	M18
R3.1.1	Interconnect driven low power high-level synthesis	3	OFFIS	REPORT	INT	M9
R3.1.2	Tool for supporting low power high-level synthesis (prelim.)	3	OFFIS	PROTOTYPE	INT	M12
R3.2	Tool for source code transformations (data path power) (prelim.)	3	OFFIS	PROTOTYPE	INT	M18
R3.3	Tool for source code transformations (memory power)	3	OFFIS	PROTOTYPE	INT	M18

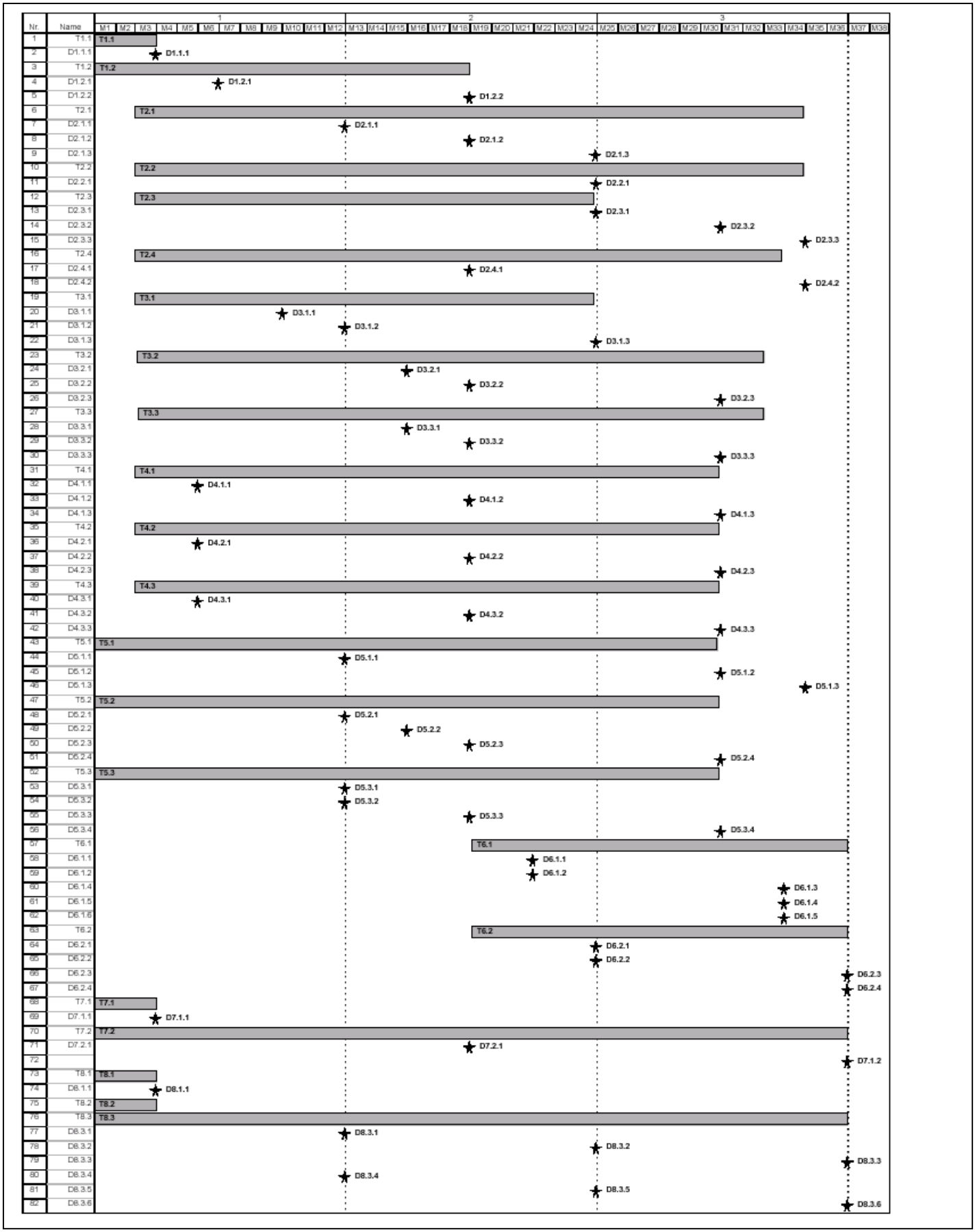
	(prelim.)					
R4.1	Tool for low-power memory and communication interface design and for dynamic power management (prelim.).	4	POLITO	PROTOTYPE	INT	M18
R 5.1	Tool with enhanced software level estimation capabilities (prelim.)	5	CEFRIEL	PROTOTYPE	INT	M18
R5.2	Tool with enhanced estimation capabilities: (prelim.)	5	OFFIS	PROTOTYPE	INT	M18
R5.3	Tool with enhanced cycle-accurate RTL power estimation capabilities (prelim.)	5	POLITO	PROTOTYPE	INT	M18
R6.1.1	Integration of algorithm and RT level prototypes (preliminary)	6	OFFIS	REPORT	INT	M21
R6.1.2	Integration of software, algorithm and RT level optimiser prototypes (final)	6	OFFIS	REPORT	INT	M33
R7.1.1	Market overview	7	OSC	REPORT	PUB	M6

9.6. List of Deliverables (distributed in consortium and to the EC)

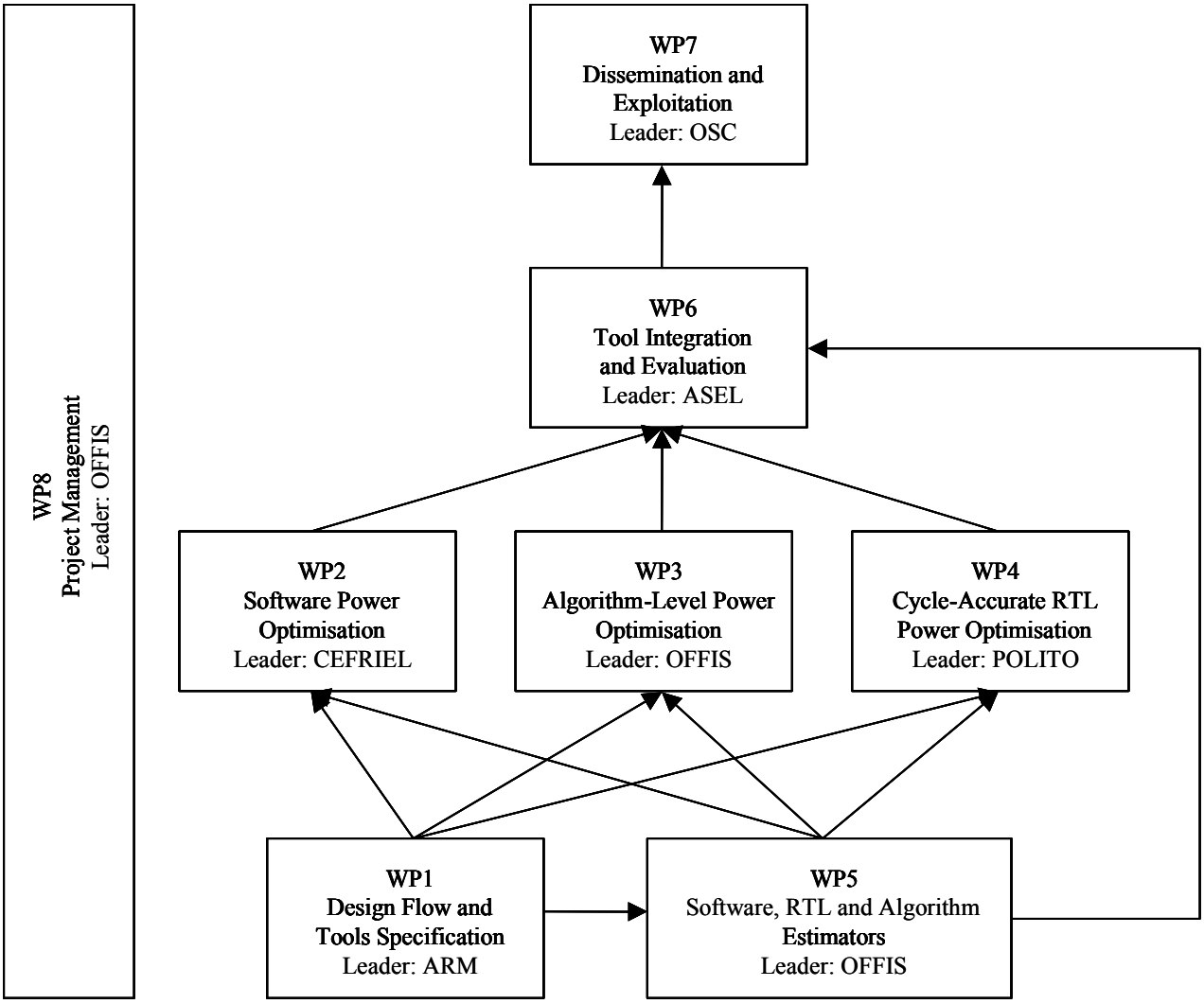
Del. No.	Deliverable name	WP No.	Lead Participant	Type	Secu-rity	Del. Date
D1.1	Specification of Design flow	1	ARM	REPORT	INT	M3
D1.2.1	Initial Specification of Tool Requirements	1	ARM	REPORT	INT	M6
D1.2.2	Refined Specification of Tool Requirements	1	ARM	REPORT	INT	M18
D2.1	Identification of main power effects related to memory management and processor architecture and related techniques for power reduction	2	CEFRIEL	REPORT	INT	M12
D2.2	Power reduction related to library and operating system calls and design guidelines at source code level	2	CEFRIEL	REPORT	INT	M24
D2.3.1	Prototype version of a tool for power optimisation of C source code	2	CEFRIEL	PROTOTYPE	PUB	M30
D2.3.2	Bug fixing and final user manuals	2	CEFRIEL	REPORT	PUB	M34
D2.4	Power models of cache architectures for embedded microprocessors	2	ARM	REPORT	INT	M34
D3.1	Tool for supporting low power high-level synthesis (final)	3	OFFIS	PROTOTYPE	PUB	M24
D3.2.1	Source transformations to minimise memory and data path power	3	OFFIS	REPORT	INT	M15

D3.2.2	Tool for source code transformations (memory and data path power)	3	OFFIS	PROTOTYPE	PUB	M30
D4.1	Techniques for low-power memory and communication interface design and for dynamic power management	4	POLITO	REPORT	INT	M12
D4.2	Tool for low-power memory and communication interface design and for dynamic power management (final).	4	POLITO	PROTOTYPE	PUB	M30
D5.1	Enhanced Tool including dynamic estimations and user manual	5	CEFRIEL	PROTOTYPE	PUB	M30
D5.2.1	Prototype tool with ANSI C/C++ front-end and enhanced behavioural power estimation kernel	5	OFFIS	PROTOTYPE	INT	M12
D5.2.2	Tool with enhanced estimation capabilities: (final)	5	OFFIS	PROTOTYPE	PUB	M30
D5.3.1	Adding cycle-accurate and dynamic capabilities to a structural RTL power estimator	5	POLITO	REPORT	INT	M12
D5.3.2	Tool for cycle-accurate RTL power estimation (final.)	5	POLITO	PROTOTYPE	PUB	M30
D6.2.1	Preliminary evaluation report issued by ASEL	6	ASEL	REPORT	INT	M24
D6.2.2	Preliminary evaluation report issued by ARM	6	ARM	REPORT	INT	M24
D6.2.3	Final evaluation report issued by ASEL	6	ASEL	REPORT	INT	M36
D6.2.4	Final evaluation report issued by ARM	6	ARM	REPORT	INT	M36
D7.2.1	Draft Exploitation Plan	7	OSC	REPORT	INT	M12
D7.2.2	Final Exploitation Plan	7	OSC	REPORT	INT	M36
D8.1.1	Project Consortium Agreement	8	OFFIS	REPORT	INT	M3
D8.2.1-D8.2.3	Periodic Progress Reports (every 12 months)	8	OFFIS	REPORT	INT	M12-M36
D8.3.1-D8.3.12	Periodic Management Reports (every 3 months)	8	OFFIS	REPORT	INT	M3-M36
D8.4.1-D8.4.3	Cost statements (every 12 months)	8	OFFIS	REPORT	INT	M12-M36

9.7. Project Planning and Timetable

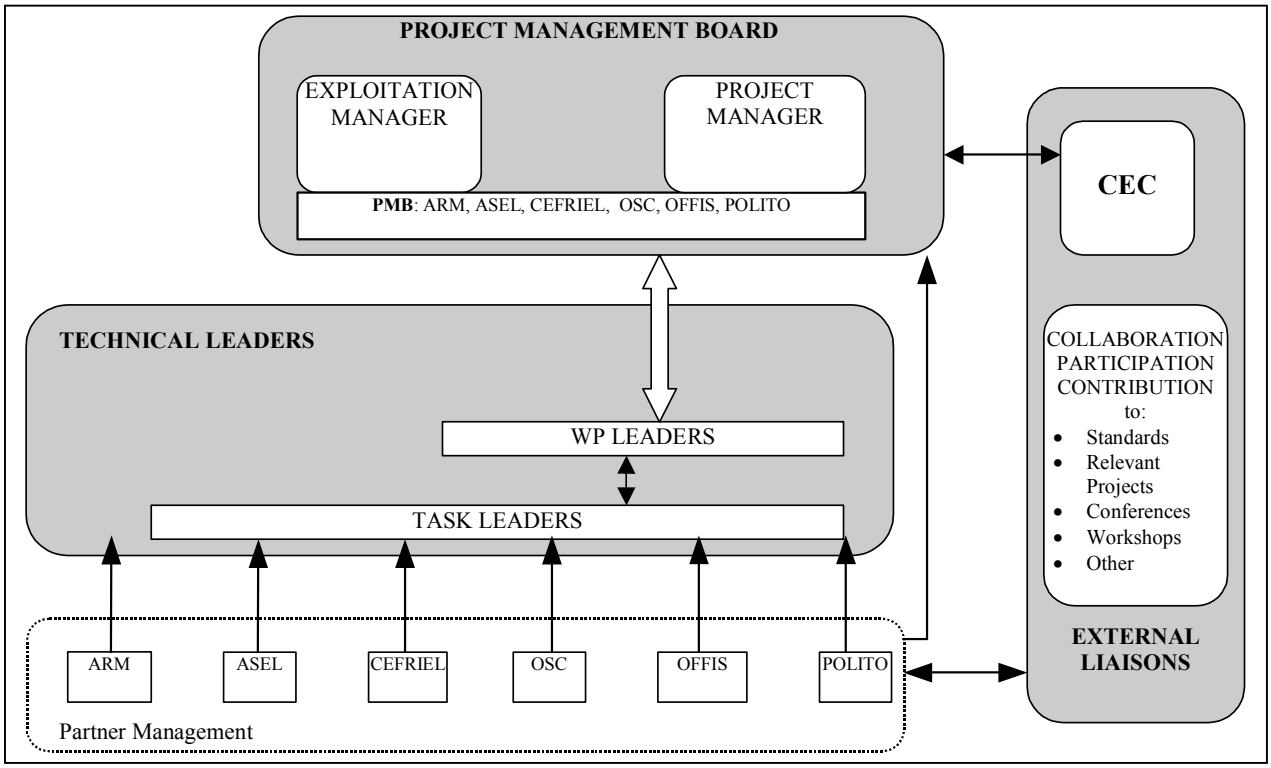


9.8. Graphical Presentation of Projects Components



9.9. Project Management

For this project, technical, exploitation, and administrative responsibilities will be shared across different management structures: Project Management Board (PMB), Project Manager (PM), Exploitation Manager (EM), Work Package Leaders (WPL) and Task Leaders (TL).



All partners in the project will participate in the management activities and will allocate a part of their manpower for management. Each partner will have a *technical representative* and a *management representative* (which can coincide). The management representative will have the authority to make decisions on behalf of his company in terms of overall strategy and resources allocated to the project. The technical representative should be able to make decisions as to the particular technical interests and how to use the resources allocated for the project.

A consortium agreement between all partners will be worked within the first three months of the project addressing preliminary recognition of background information and access rights and conditions; responsibilities and obligations between partners in case of withdrawal or non performance.

9.9.1. Project Management Board (PMB)

The PMB will be composed of one management representative from each partner in the consortium and the project manager. The role of the PMB will be:

To set up the overall direction of the project. This includes discussing and proposing major changes in the work plan in response to new problems or new situations.
To review EDA tools and techniques related to the project.
To set up the consortium agreement.
To approve major modifications to project plans.

To set up arbitration policies.

The board will be chaired by the project manager and will meet at least once every 6 months. The meetings will be convened either periodically or at the request of any of its members. Meetings can also be held as phone-conferences. The decisions will be taken by consensus or by simple majority in the case where consensus is not possible. Changes to the work plan in the proposal will require consensus or a qualified majority of all except one. A project manager, who is not the representative of the co-ordinating partner, will not vote. The project manager will resolve any tie in the vote.

9.9.2. Project Manager

The co-ordinator will take the role of the Project Manager. The PM reports to the PMB and to the Commission. The role of the Project Manager will be to:

To co-ordinate all activities and detect deviations. The PMB will be involved if necessary.
To convene the PMB.
To monitor project progress and workload consumption.
To keep partners informed about project progress.
To manage reporting to the Commission and serve as the administrative liaison with the Commission.
To prepare and follow-up PMB meetings.
To serve as project secretary and archive.

9.9.3. Exploitation Manager

The exploitation manager (EM) will be responsible for the on-going management of the project exploitation activities. He will draw together exploitation possibilities for POET results as a whole, with the aim of exploiting these results as a product or set of products. He will continuously observe the development of the POET target market in order to provide an early feedback and initiate corrective actions when required.

9.9.4. Workpackage Leaders

The WP leaders will be appointed by the partner responsible. The role of Workpackage Leaders (WPL) will be to:

To co-ordinate activities in the WP and ensure communication among the participants, especially among the TL.
To initiate corrective actions for deviations.
To ensure the well timed availability of WP deliverables.
To report progress to the Project Manager and PMB.
To co-ordinate the interaction and collaboration with other WPs.
To convene WP meetings.
To arrange technical reviews as required by the PMB or the Commission.

9.9.5. Task Leaders

The task leaders will be appointed by the WPL in co-ordination with the executing partner. Their role is to co-ordinate the task activities. They report to the WPL.

10. Clustering

The industrial acceptance of low power design tools requires the proven efficiency and compatibility with standard practice. It is thus of key interest of the project to co-operate with other projects and activities inside and outside the EU in order to continuously disseminate information about POET to the rest of the world, to influence developments in the interest of the consortium, and to adjust the target to new trends and developments. The prime strategy of the consortium is to participate in this process through OSC, however, in addition any other opportunity will be explored.

11. Other contractual conditions

POLITO will subcontract to CFR some of the work in Tasks T4.3 (8 PM) and T5.3 (10 PM), for a total of 18 mm.

The breakdown of the subcontract over the project lifetime is the following:

Year 1: 7 PM
Year 2: 7 PM
Year 3: 4 PM

The costs to be covered by the subcontract are personnel costs only.

OSC will subcontract to BullDAST some of the work in WP7 for a total of 24 mm, equally distributed over the project lifetime (i.e., 8 person month per year). The costs to be covered by the subcontract are personnel costs (90% of the subcontracted budget) and other specific costs related to the participation to exhibits and fairs of BullDAST (10% of the subcontracted amount).

Appendix A : Consortium Description

To achieve the goal of the project, a consortium with a well-recognised background and specific competence has been put together. The consortium was constructed by taking into account that co-operation is crucial and that all partners must have a clear role that leads to good technical, exploitable results. Each partner has a clear business area orientation in the project.

The members in the consortium are:

Company	Role	Key Areas in the Project
OFFIS	Project Leader, Tool Developer	Project Coordination and Management Algorithmic Level Power Optimisation and Estimation
CEFRIEL	Tool Developer	Software Level Power Estimation and Optimisation
Politecnico di Torino	Tool Developer	Cycle Accurate RTL Power Estimation and Optimisation
ASEL	Tool User, Engineering Know How	Requirements Specification, Specification and Evaluation of Methodology and Tools in its application domain: high complexity high speed ASICs
ARM	Tool User, Technology Provider Developer	Requirements Specification, Specification and Evaluation of Methodology and Tools in its application domain: low power processor cores. Provide technology . Support CEFRIEL in software power optimisation
OSC	EDA tool vendor	Tool Exploitation and Dissemination

Table 1. Complementary Aspects of the Consortium

The partners have experience in many different areas and have previously worked together on several European projects. Most partners have been successfully working together on the IST Project PEOPLE dealing with the development of prototype tools for power estimation of SoCs.

As stated before, NOKIA and Siemens ICN have expressed their strong interest in this project and assured to help in the definition of the requirements and in the evaluation phase in a less formal way (See the included letters of interest at the end of this document)

A.1 Kuratorium OFFIS e.V. (OFFIS), Germany

OFFIS, the “Oldenburger Forschungs- und Entwicklungsinstitut für Informatik-Werkzeuge und Systeme”, is a non-profit state funded research institute associated with the University of Oldenburg (FRG). OFFIS currently employs some 90 full time graduate or post-graduate computer scientists and is expected to grow to up to 120 scientists during the next few years. OFFIS is organised into four R&D divisions, one of them being dedicated to Embedded Systems.

OFFIS successfully participated in a number of EU projects including: FORMAT, REQUEST ,SACRES, VIP and SQUASH. Further OFFIS participated in Low Power related projects of the

JESSI and MEDEA programmes, namely JESSI-AC8 and MEDEA EURIPIDES. Currently the division is contributing to the IST projects VIP and ODETTE and the 4th framework project PEOPLE. The focus of these projects is on power optimisation of embedded systems and system-level design automation.

In the POET project, OFFIS will be responsible for algorithmic and memory power estimation and optimisation as well as associated tools, their implementation, and technology transfer. OFFIS also has a well-recognised background and competence in project management and will act as the coordinator.

The scientific supervision of the POET project inside OFFIS will be done by Prof. Dr. Wolfgang Nebel. Since 1993 he is Professor at the Computer Science Department of the University Oldenburg. He started first work on power estimation during his responsibility as CAD software development manager of Philips Semiconductors Hamburg. He is involved in the low power community as general chair of the PATMOS workshop 1995 and program chair at PATMOS'96; PATMOS is the dedicated European event for power and timing modelling. Dr. Nebel was director of the NATO advanced study institute Low Power Design in 1996. He was programme chair of EURO-VHDL 1994 and 1995, programme chair of EURO-DAC 1996 and 1997, programme co-chair of DATE98 and is currently program chair of DATE 2001. He is a member of the advisory board of the Kluwer Academic Press "Current Issues in Electronic Modelling" and several other design automation related program committees. He is member of IFIP 10.5, IEEE, ACM, and GI.

A.2 CEFRIEL, Italy

CEFRIEL is a consortium between University and Industry in the Milan area that was founded in early 1989. It is devoted to both research and education in the field of Information Technology (computers and communication). Both advanced (post graduate Master courses) and permanent educational activities are targeted together with cooperative research activities oriented to medium/long term applications. Research is pre-competitive and the sponsor industry participates with tools and employees who perform part-time research at Centre’s premises. The close collaboration of industry representatives and CEFRIEL researchers in an environment that has the capability to support a broad range of R&D activities will also avoid many of the pitfalls associated with sequential technology transfer.

The Centre's research and development activities are organized around eight research areas and several European and national projects. The area interested in the proposal is called ESD (Embedded Systems Design area), whose initial focus has been on the HDLs and hardware design. Since 1993 the main activity of the research group is in the field of HW/SW codesign, of embedded systems, where the previous experience in hardware design has been capitalized and extended in order to cover also software related issues. A significant effort has been devoted to the problem of design space exploration, system level cosimulation of mixed HW/SW architectures, power analysis and optimisation both for hardware and software specifications and modelling of the cost-effectiveness of IP reuse. Part of these investigations has been carried out during the projects PEOPLE and SEED, founded by the EU.

In the POET project CEFRIEL will be responsible for the development of the prototype tools for software power estimation and optimisation.

The scientific supervision of the POET project inside CEFRIEL will be done by Donatella Sciuto received her Laurea in Electronic Engineering in 1984. She received her PhD in Electrical and Computer Engineering in 1988 from University of Colorado, Boulder. She has been an Assistant Professor at the University of Brescia, Dipartimento di Elettronica per l'Automazione until 1992. She is currently a Full Professor at the Dipartimento di Elettronica e Informazione of the Politecnico di Milano, Italy. She is member IEEE, IFIP 10.5, SIG-HDL,

EDAA. She is member of different program committees of EDA conferences: DAC, ICCAD, DATE, CODES/CASHE, DFT, FDL, and associate Editor of the Journal Design Automation of Embedded Systems, Kluwer Academic Publishers. She has participated and coordinated a number of European and industrial funded projects in the area of electronic design automation. Her research interests cover the methodologies for hardware/software co-design of embedded systems, from the specification level down to the implementation of both the hardware and software components.

A.3 Politecnico di Torino (POLITO), Italy

The EDA group in the Dipartimento di Automatica e Informatica has long been active in the development of prototype CAD tools for the automatic synthesis of VLSI circuits and systems. In particular, noticeable results have been achieved in the last few years in the areas of gate, RT, and behavioural-level power modelling, estimation, and optimisation, as demonstrated by the list of technical articles published on the major journals and conference proceedings. The group comprises a total of seven professors, and a number of Ph.D. and undergraduate students. Funding for the group has been attracted from industrial contracts, the Italian National Research Council, the Italian Ministry for University and Scientific Research and the European Commission through a number of ESPRIT projects, including the PEOPLE project.

In the POET project, Politecnico di Torino will be responsible for the development of the prototype tools for cycle-accurate RTL power estimation and optimisation.

The technical supervision of the POET project inside Politecnico di Torino will be done by Prof. Enrico Macii, who received the PhD degree in computer engineering from Politecnico di Torino. From 1991 to 1994 he was an Adjunct Faculty at the Dept. of Electrical and Computer Engineering of the University of Colorado at Boulder. Currently, he is an Associate Professor of Computer Engineering at the Dip. di Automatica e Informatica of Politecnico di Torino. Enrico Macii is an Associate Editor of the IEEE Transactions on CAD and an Associate Editor of the ACM Transactions on Design Automation. In 1999, he was the Technical Program Co-Chair of the IEEE Alessandro Volta Memorial Workshop on Low-Power Design, in 2000 he was the Technical Program Co-Chair of the ACM/IEEE Intl. Symposium on Low-Power Electronics and Design, and in 2001 he will be the General Chair of the same event. He has published over 200 technical articles in international journals, books and conference proceedings. He was the technical manager inside Politecnico di Torino of the PEOPLE project.

CFR (POLITO’s subcontractor)

Consorzio Ferrara Ricerche (POLITO's subcontractor) is a non-profit organization whose purpose is to promote and support specific research projects concerning several fields, including health, environment, biotechnologies, and information technology. Most of the internal personnel (staff and research) belongs to academic institutions, mainly University of Ferrara and University of Bologna.

CFR invests all his revenues to provide scholarships in academic institutions, to buy durable equipments for research labs, and to organize cultural and educational events.

In the POET project, CFR will be responsible for the development of power models for RTL macros to be used in the context of automatic insertion of power-management circuitry (Task 4.3) and for the development of cycle-accurate power estimation capabilities (Task 5.3).

The technical contact within CFR for the POET project is Dr. Alessandro Bogliolo, who received the Laurea degree and Ph.D. in Electrical Engineering from University of Bologna in 1992 and 1998, respectively. From 1992 to 1999 he was with the Electronics, Computer

Science and Systems Department of University of Bologna, and from 1999 to 2000 he was a Senior Researcher at Politecnico di Torino. He was also a Visiting Scholar at the Computer System Laboratory at Stanford University in 1995 and 1996. In 2001, he joined the Department of Engineering at the University of Ferrara as an Assistant Professor. His research interests are in the area of computer-aided design of digital integrated systems, with special emphasis on high-level power modelling and power optimisation. While at Politecnico di Torino, he cooperated to the ESPRIT project n. 26796 PEOPLE on the development of power models for hard and soft macros.

A.4 Alcatel SEL (ASEL), Germany

Alcatel SEL is the German subsidiary of Alcatel Telecom, on of the world's largest manufacturers of telecommunications systems. The microelectronics department in Stuttgart belonging to the Alcatel Switching & Routing Systems Division (SRD) has strong expertise in the area of advanced VLSI components for all types of telecommunications systems. The VLSI circuit development covers transmission, switching, ATM, mobile and access applications. Advanced design methodologies, strong links to other European Alcatel microelectronic design centres, as well as a frequent participation in research projects, are key elements of the department's development strategy.

In the POET project ASEL will be responsible for the specification of the design flow and tool requirements and for the industrial evaluation of the developed tools.

The technical supervision of the POET project inside ASEL will be done by Jürgen Meyer who studied Computer Science at the University of Oldenburg in Germany from 1991 till 1997. During his studies he concentrated on theoretical and technical computer science, i.e. computer architectures, multiprocessor systems, formal verification and modelling. After passing his examination with distinction and receiving his masters degree, he started his career at the microelectronic centre of the Switching & Routing division of Alcatel SEL in Stuttgart, Germany. There he is working as a developer in the top-level and ASIC design team. His expertises cover system modelling, embedded system design and methodology and tools for HW/SW co-design, co-simulation and co-verification. In addition he was responsible for the coordination and technical leadership of the Esprit project PEOPLE inside ASEL.

A.5 ARM Limited (ARM), U.K.

ARM is one of the world’s leading intellectual property (IP) providers, and is an extremely successful European company with a quoted stock market value of more than €8bn. ARM develops and licenses high-performance, low-cost, power-efficient RISC (reduced instruction set) processors and cores, peripherals, and system-chip designs to leading international electronics and systems design and integration companies. ARM also provides a comprehensive support environment required in developing a complete system. ARM's microprocessor cores are rapidly becoming the volume RISC standard in such markets as portable communications, hand-held computing, multimedia digital consumer products and embedded system. From just 12 employees at its start-up around 10 years ago, ARM now employs more than 600 people world-wide – more than 450 of them in the EU – including some of the best processor and software design engineers in the world. ARM serves its growing partnership base from its main offices in Cambridge, Sheffield and Maidenhead in the UK and from several European offices. Additional offices are in Los Gatos, California; Austin, Texas; Seattle, Washington; Northborough (MA), USA; Tokyo, Japan, Taiwan and Seoul, Korea. More information on ARM is available at http://www.arm.com.

The development of the ARM microprocessor architecture has been a highly successful undertaking. Several of the key stages of its development have been accomplished in conjunction with EC projects and with other leading European development organisations.

The ARM processor is licensed by more than 40 partner and semiconductor foundries worldwide and designed-in to more than 600 products.

The technical supervision of the POET project inside ARM will be done by Tim Hopes, who is the Engineering Manager of the Modelling and Debug Solutions Group, responsible for managing the ARM Ltd. EDA engineering team and newly formed Debug Solutions engineering group (debug targets and debuggers). The EDA group comprises more than 40 engineers across 5 sites, mainly in the UK and USA. In a previous position, Tim was Engineering Manager of the ARM's EDA Business Unit, commercially directing around 20 engineers developing leading edge models of ARM CPU cores. Prior to this, Tim was the European Technical and Product Marketing Manager for Synopsis, responsible for verification products including modelling products, logic emulators and telecommunications workbenches. Tim has also worked for Modeling Corp., modelling of processors and ASSPs, and spent six years at Intel as a design engineer providing design and end-user support for ASICs including 8031 and 80186 embedded processors, and three years as a design engineer at Marconi Communications. Tim has an Honours Degree in Electronic Engineering from the University of Southampton and is a holder of the Diploma of Engineering.

A.6 OSC, Germany

OSC GmbH was founded 1999 in Oldenburg, Germany. As a spin-off company to OFFIS, an internationally renowned research institute associated with the University of Oldenburg, it combines leading edge technology know-how with a commitment to aggressively enter the market in its expert areas, currently focusing on business applications, geographical information systems and embedded systems. OSC's embedded systems LOW POWER-technology is developed in cooperation with OFFIS and patents are pending. OSC's embedded systems VERIFICATION and VALIDATION-technology is developed in cooperation with major US-based and European partners in the automotive, avionics and train systems markets. Key customers are Daimler Chrysler, BMW, Nissan and Peugeot S.A. who are implementing our technology in their software development process. Our mission is to increase product quality and reduce design time by introducing advanced LOW POWER-technology into the systems and software development process. We are offering leading edge LOW POWER-technology to the embedded systems market. Although OSC was founded only two years ago we could rapidly increase our skilled manpower situation in the benefit of our clients.

In the POET project OSC will be responsible for the commercial exploitation of the developed tools. The technical part of the exploitation of the tools developed by CEFRIEL and Politecnico di Turino will be subcontracted to BullDAST (Design Automation Services and Tools) s.r.l., established in 2000 (a company whose primary mission is that of engineering, exploiting and commercialising EDA tools developed as research prototypes by the EDA group of Politecnico di Torino). The following figure shows the organisational structure of OSC:

BullDAST s.r.l. (OSC's subcontractor)

BullDAST s.r.l., established in 2000, is a company whose primary mission is that of engineering, exploiting and commercialising EDA tools developed as research prototypes by the EDA group of Politecnico di Torino. CEO of the company is Mrs. M. C. Avalle. The internal workforce for product development and distribution is complemented by part-time personnel and consultants from the department of Electrical Engineering and from the department of Computer Engineering of Politecnico di Torino that provide technology and strategic advising.

Several semiconductor companies and system houses world-wide, including Alcatel, ARM, Infineon, Intracom, National Semiconductors, Samsung Electronics of Korea and ST

Microelectronics, have joint partnerships with BullDAST and/or rely on BullDAST design automation services.

Design support and training are additional services BullDAST offers to its customers. These include tool integration in internal design flows, enhancement of scripting capabilities, heterogeneous tool interfacing and advanced technology dissemination.

In the POET project, BullDAST will be responsible for the exploitation of the prototype tools developed by Politecnico di Torino (RTL power estimator and optimiser) and by CEFRIEL (software power estimator and optimiser).

The technical contact within BullDAST for the POET project is Dr. Riccardo Scarsi; he received the Dr. of Eng. degree in Electronics from Politecnico di Torino in 1997, and the PhD degree in Computer Engineering from the same institution in 2000. His working interests include several aspects of the development of methods and algorithms for power estimation and optimisation. Dr. Scarsi is a member of the IEEE and of ACM/SIGDA. In his scientific carrier, he has published over 50 papers in international journals (including IEEE Trans. on CAD, IEEE Trans. On VLSI Systems and IEEE Design and Test) and conferences (including DAC, ICCAD, DATE and ISLPED).

Appendix B : Contract Preparation Forms

Will be generated from Excel Files and PDF-Forms