Flip-flops

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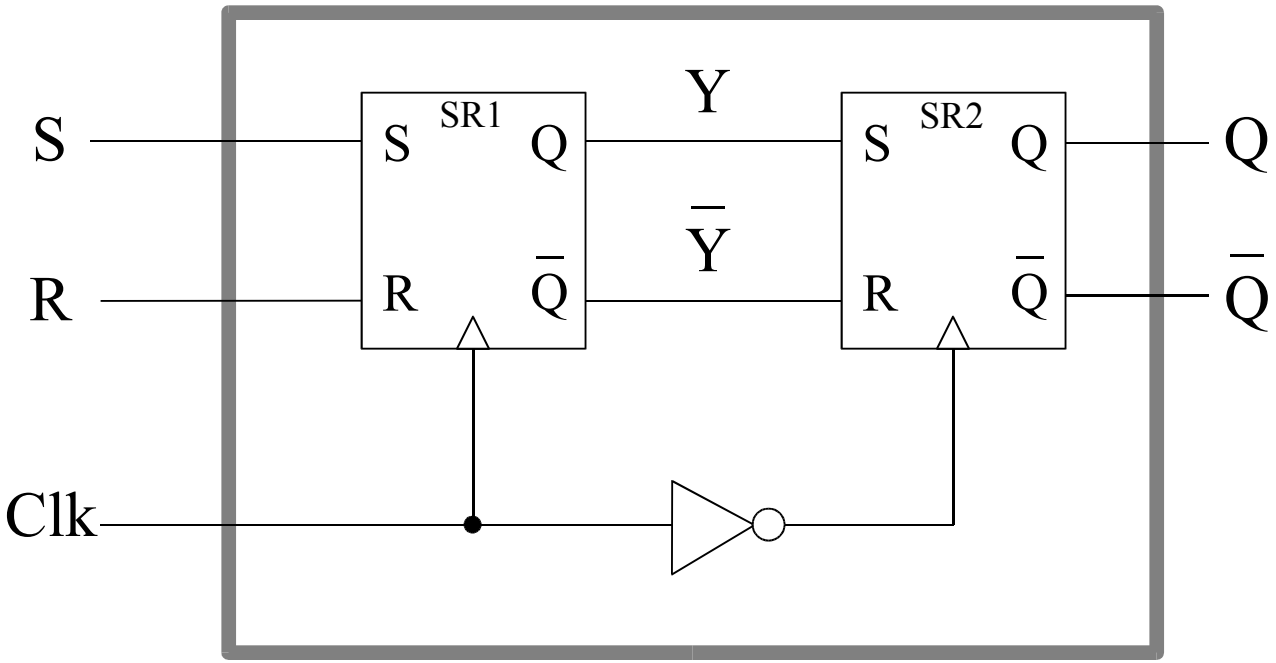
(sorry, ‘english’ is cheaper than ‘italian with english terms’)

The master-slave SR flip-flop

Structure: 2 SR synchronous latches;
1 not gate;

Total cost: 4 nor + 4 and + 1 not
(+1 not for D version)



The master-slave SR flip-flop

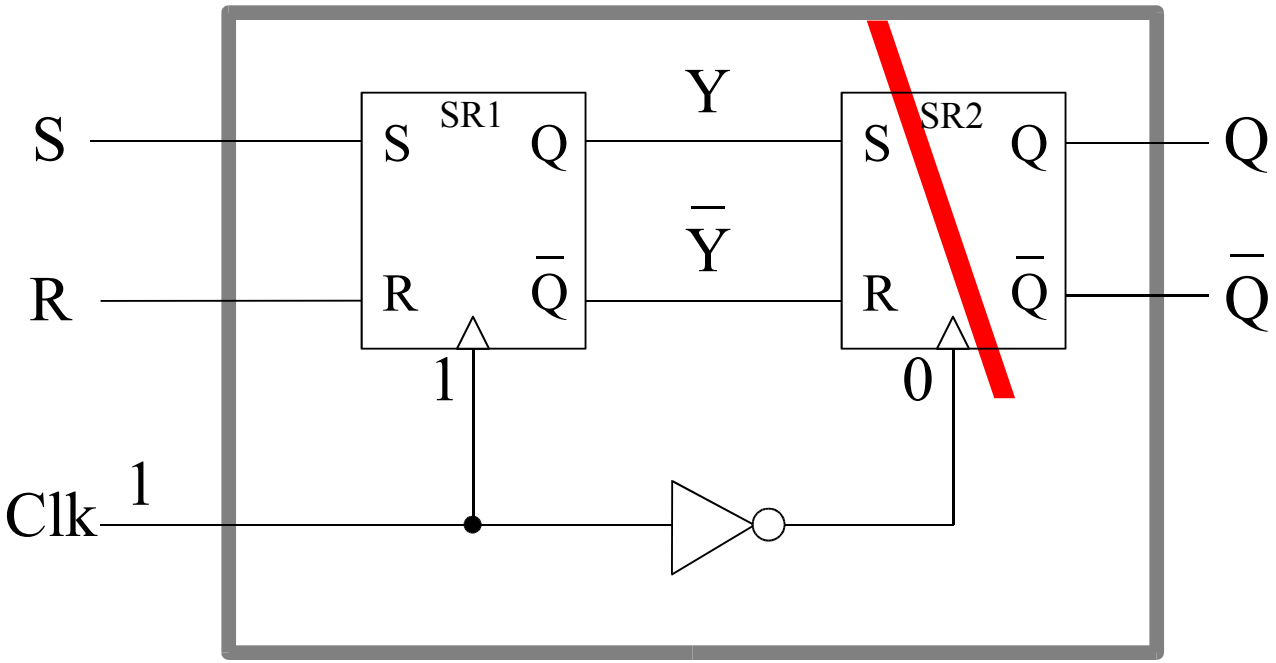
Clock=1

SR1: transparent

SR2: opaque

S, R affect Y/!Y

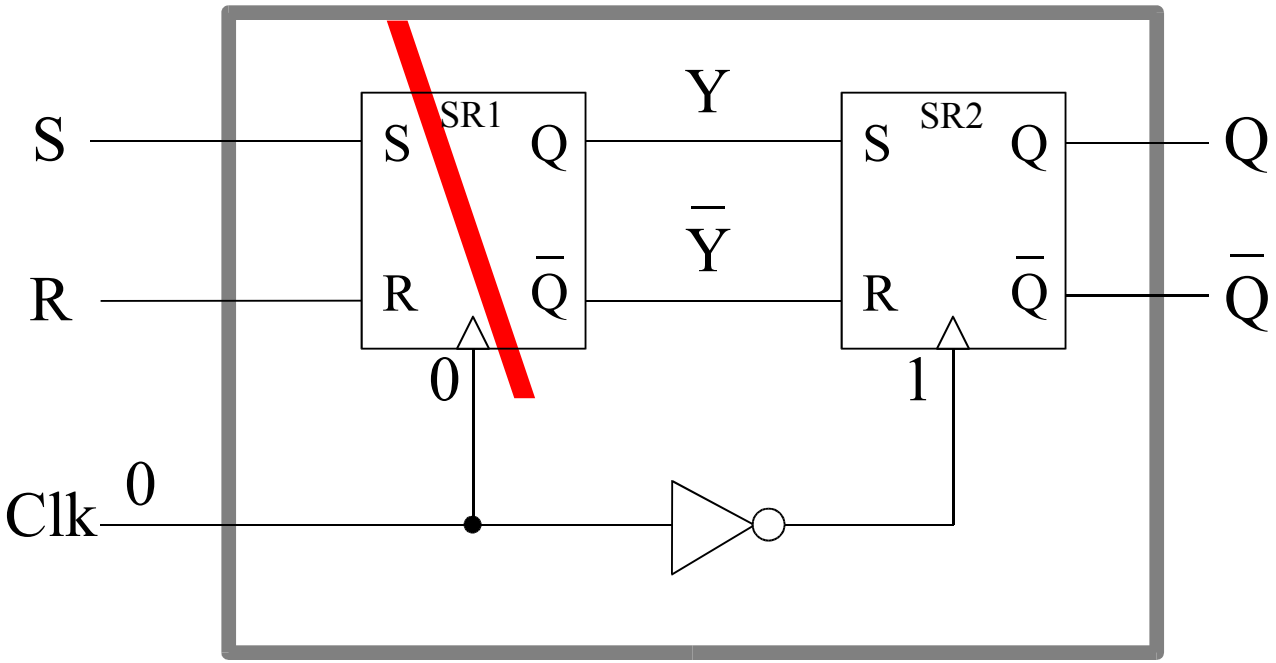
Q/!Q are unaffected



The master-slave SR flip-flop

Clock=0 SR1: opaque S, R do NOT affect Y/!Y

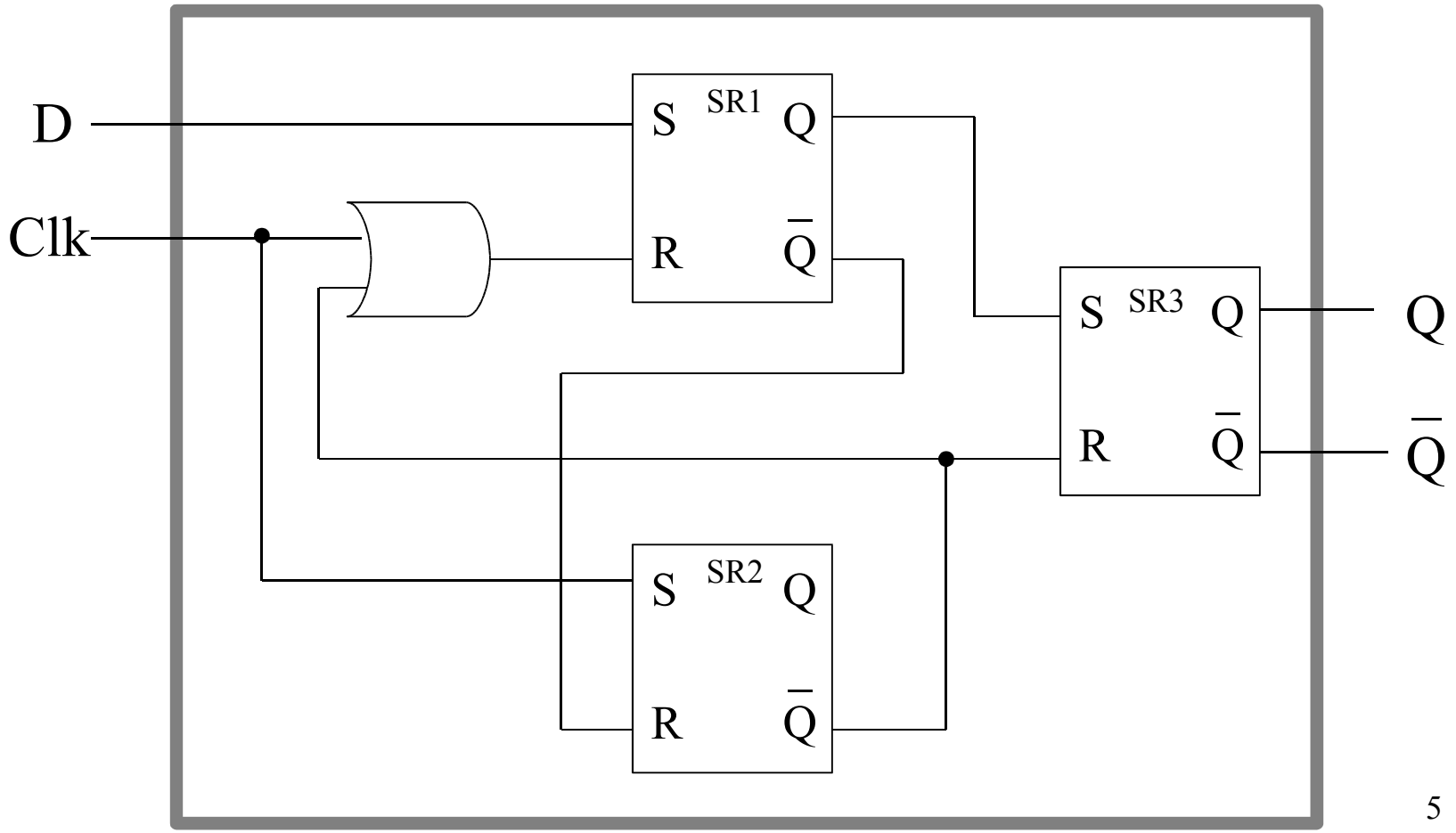
SR2: transparent Y/!Y affect Q/!Q



The edge-triggered D flip-flop

Structure: 3 SR asynchronous latches;
1 or gate;

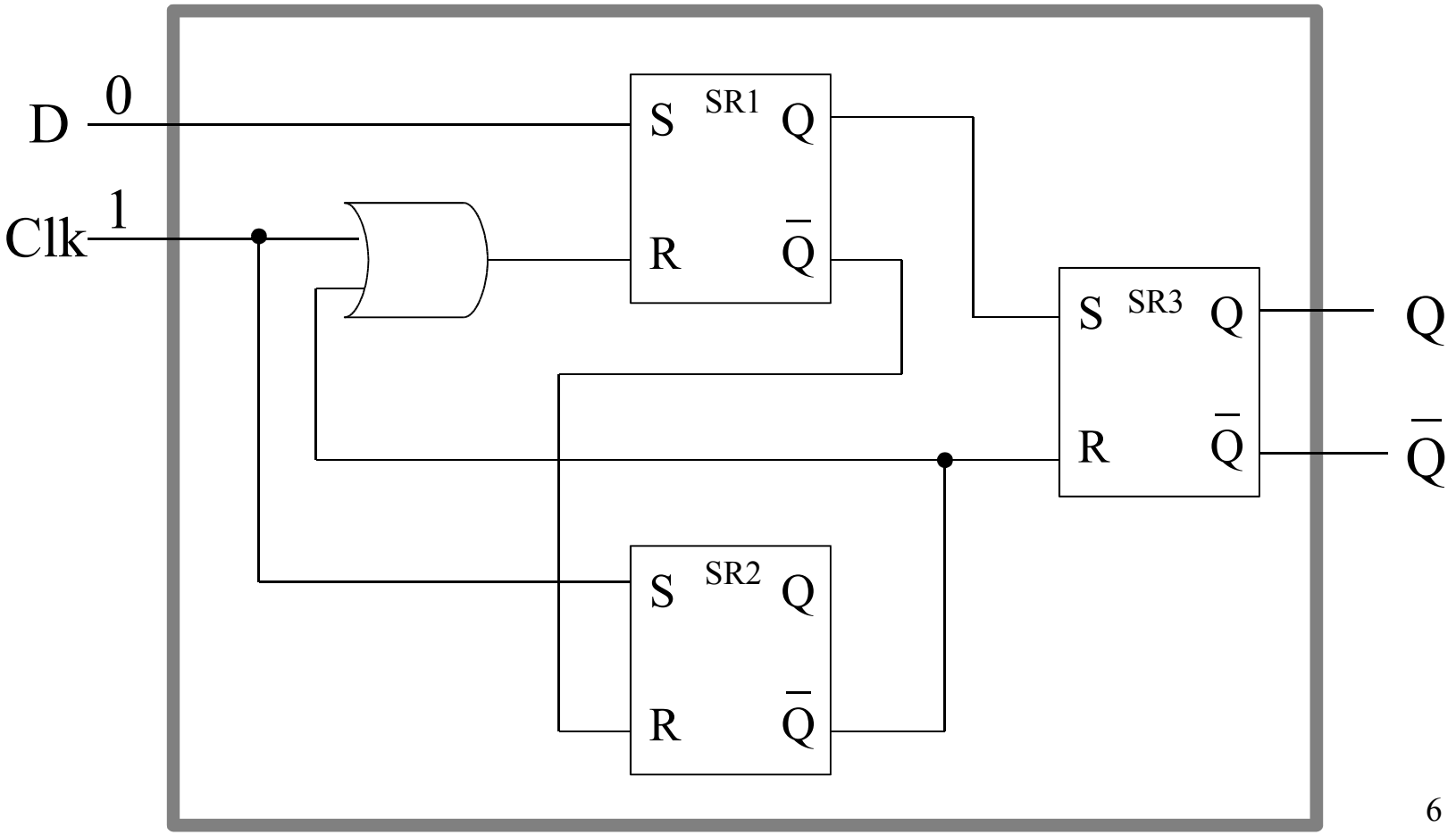
Total cost: 6 nor + 1 or (cheaper than master-slave!)



The edge-triggered D flip-flop

Case 0: Clock = 1

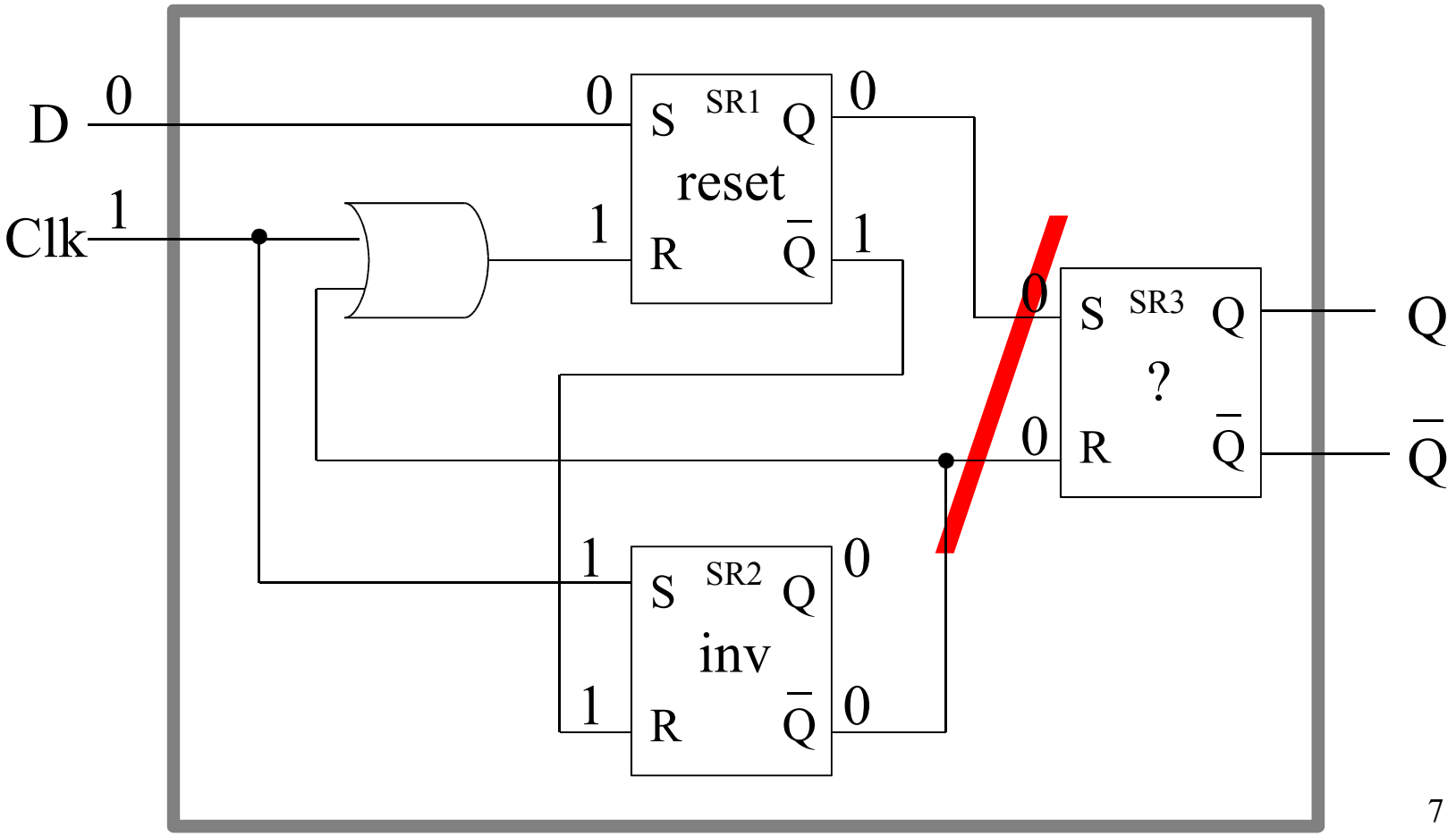
Data = 0



The edge-triggered D flip-flop

Case 0: Clock = 1 SR1: valid, 0 SR3: unaffected

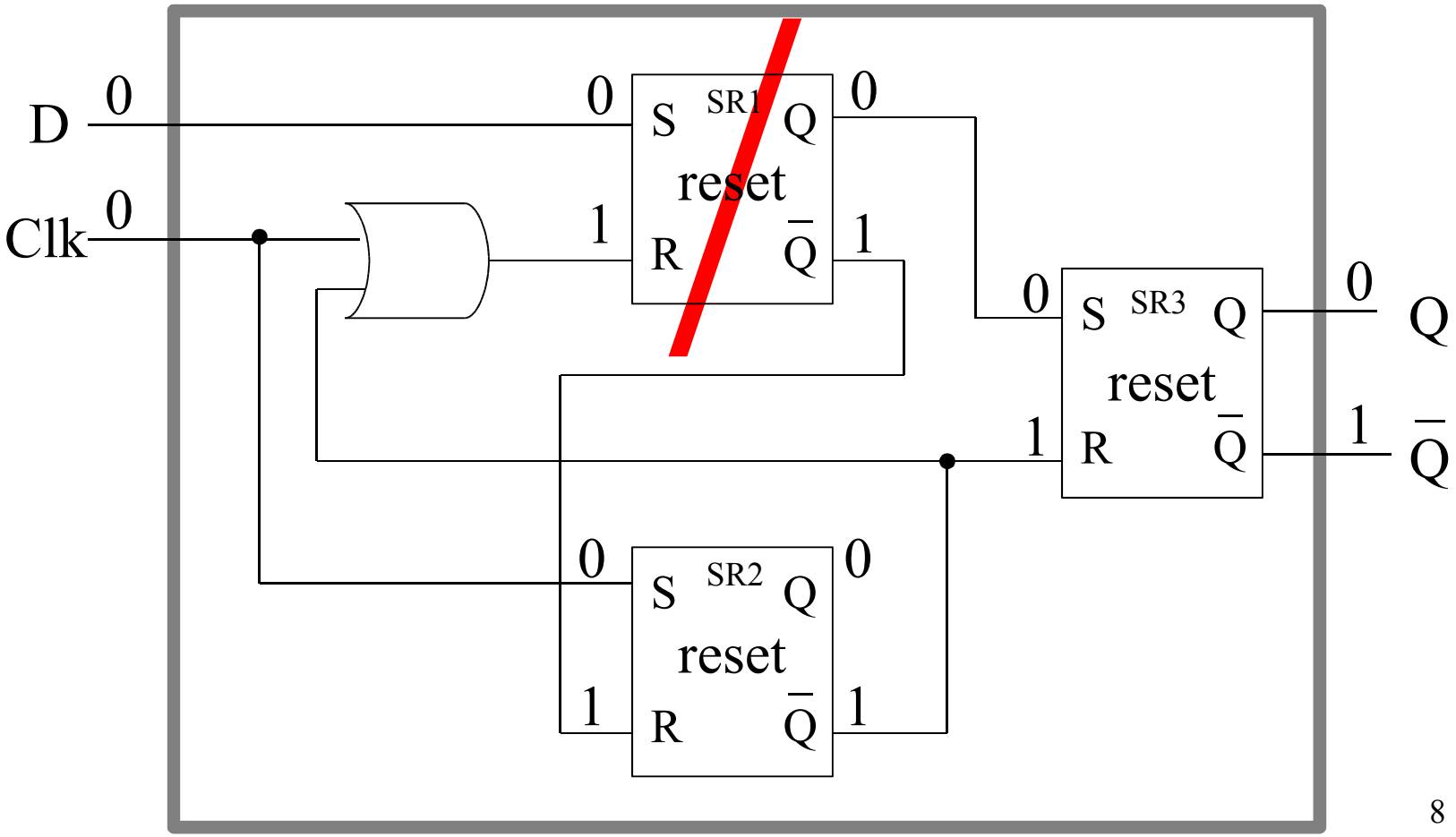
Data = 0 SR2: invalid (prev state)



The edge-triggered D flip-flop

Case 0+: Clock = 0 SR1: prev, 0 SR3: reset

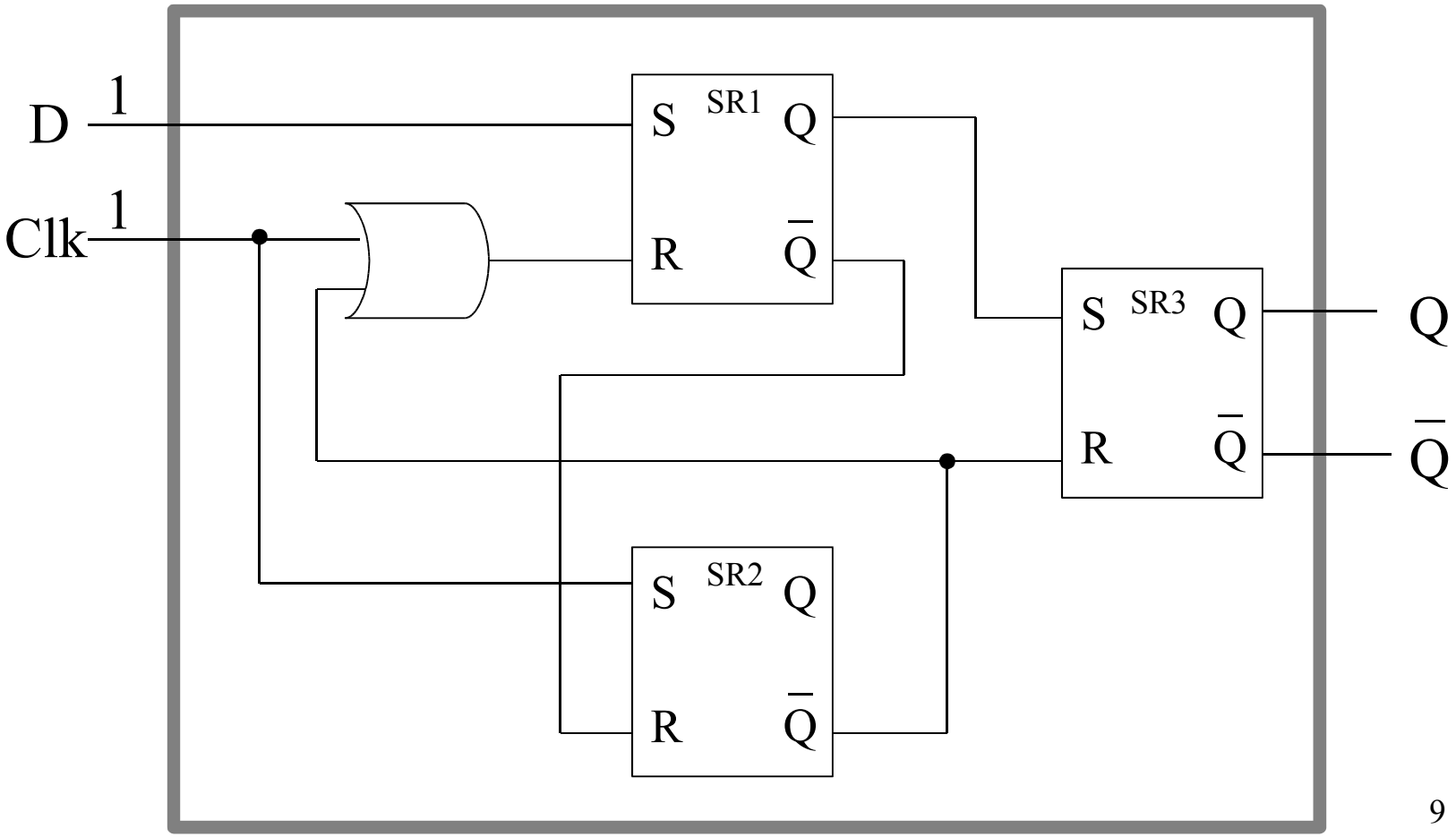
Clock down Data = 0 SR2: reset



The edge-triggered D flip-flop

Case 1: Clock = 1

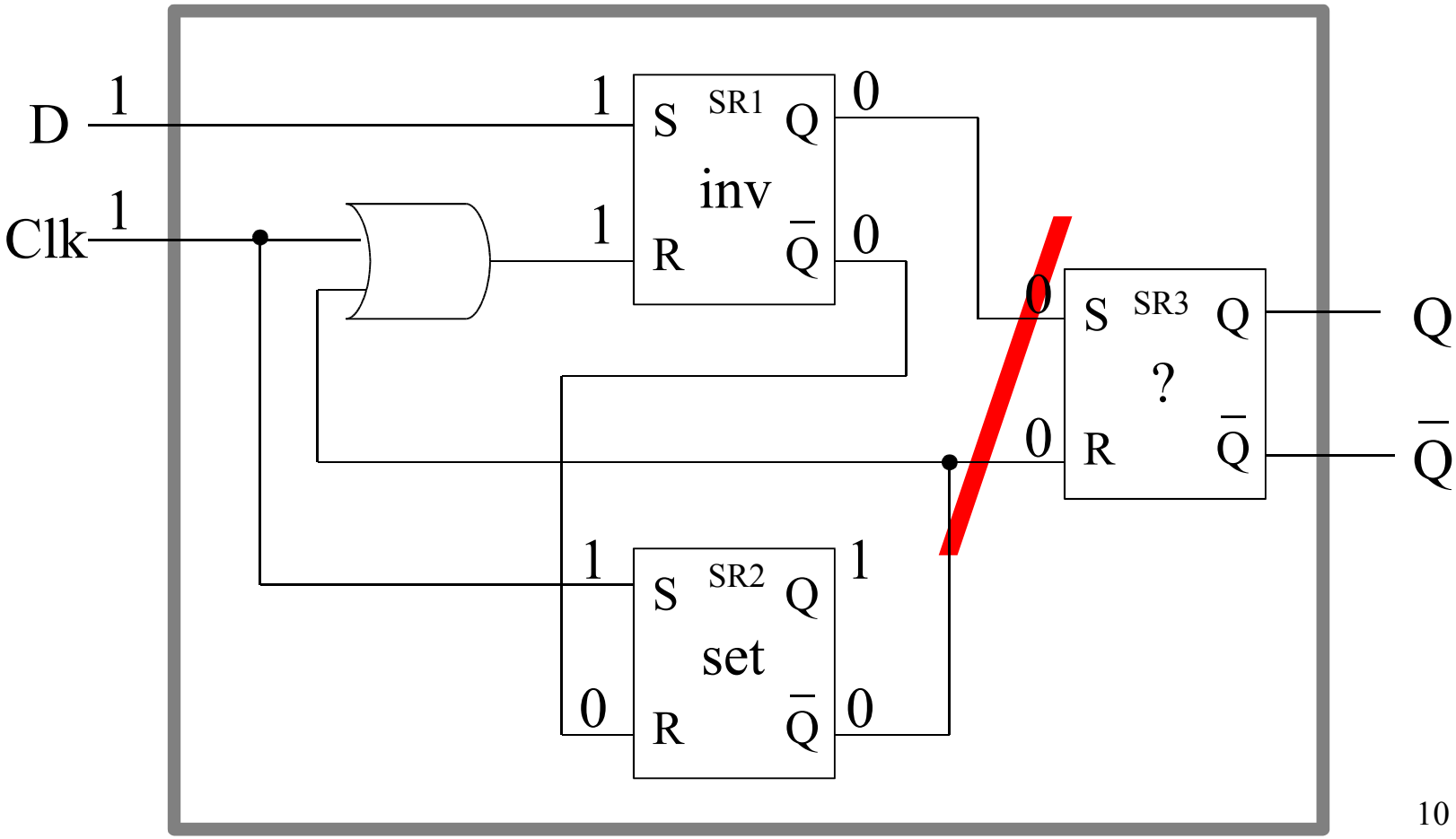
Data = 1



The edge-triggered D flip-flop

Case 1: Clock = 1 SR1: invalid SR3: unaffected

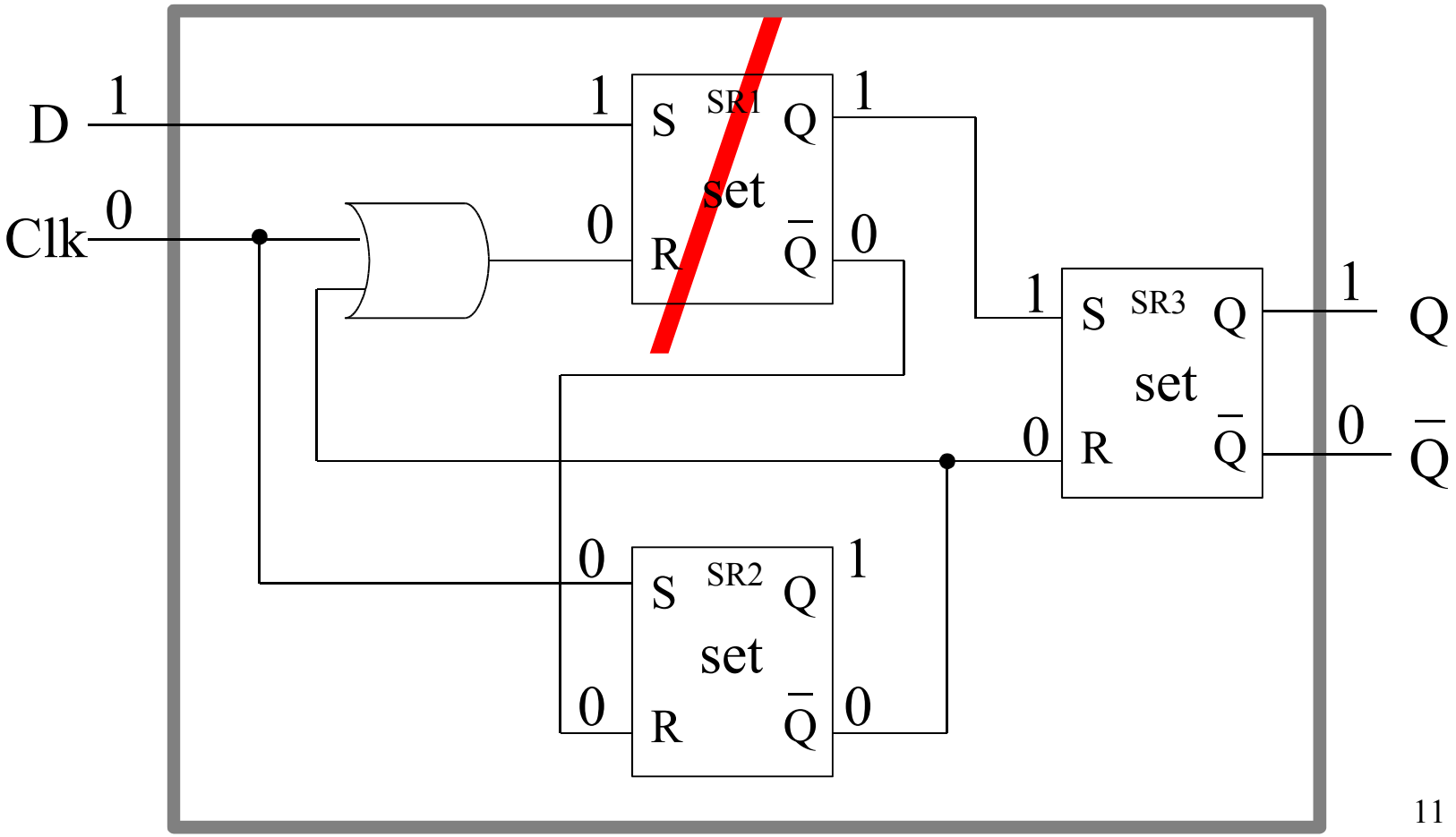
Data = 1 SR2: prev, 1 (prev state)



The edge-triggered D flip-flop

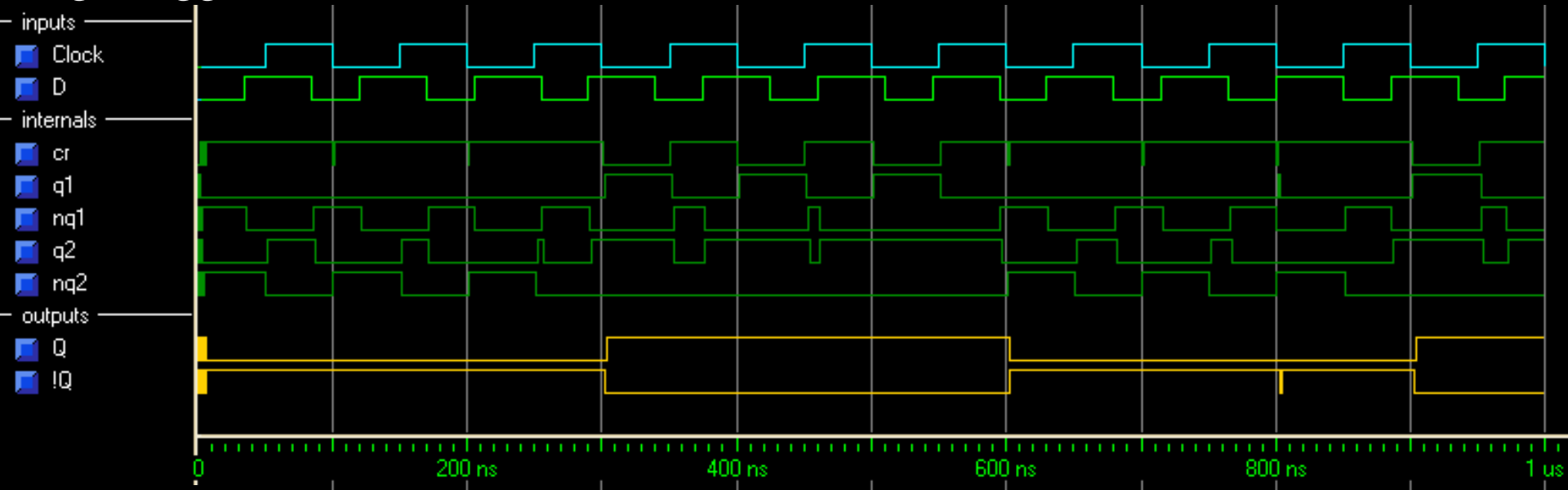
Case 1+: Clock = 0 SR1: valid, 1 SR3: set

Clock down Data = 1 SR2: prev, 1

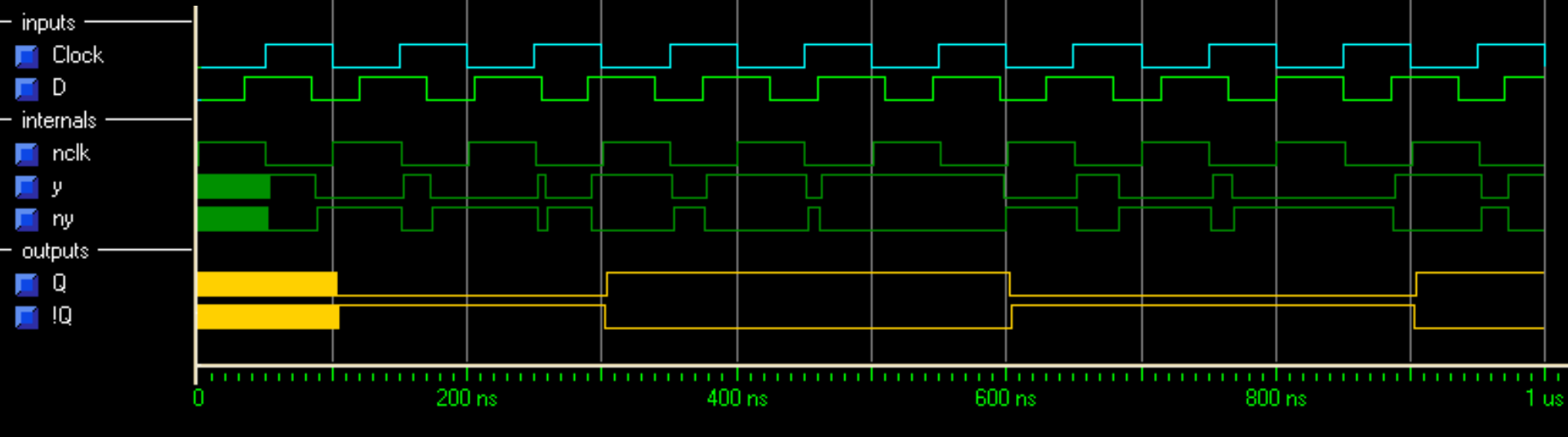


Master-slave vs. edge-triggered

Edge-triggered



Master-slave



Master-slave vs. edge-triggered: conclusions

The master-slave and the edge-triggered flip-flops are externally **IDENTICAL!**

Both sample the input signals at clock negative edge, and make it available at output.

Forget fig. 15, page 84.

Do-it-yourself logic simulation

1. Download MXE: “Modelsim Xilinx Edition” at:
   www.xilinx.com/xlnx/xil_prodcat_product.jsp?title=modelsim_xe

2. During installation request a free license;

3. Download
   scarpaz.vhd
   scarpaz.tcl
   and copy in dir:
   examples

4. Type:
   source scarpaz.tcl
   init

   dff
   dffet3